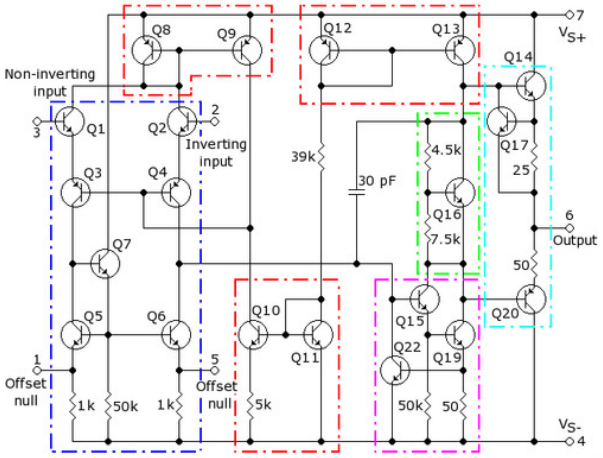
Analog Integrated Circuits

1. Name the building blocks inside the op amp shown in the figure.

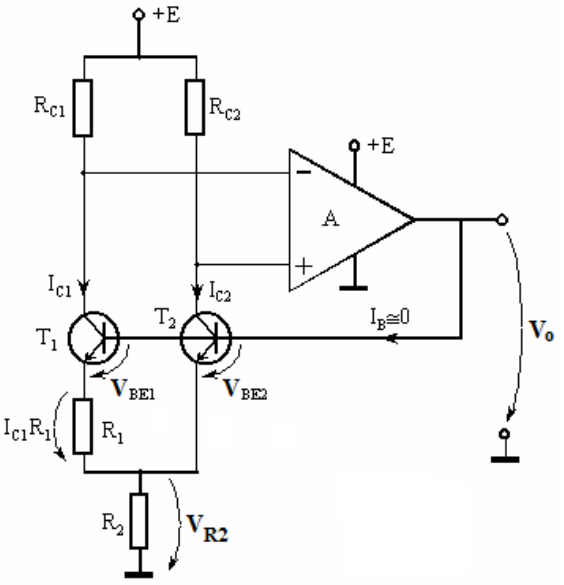


2. A band-gap-referenced bias circuit is shown in the figure. T1 and T2 are identical. The ratio of R_{c1} to R_{c2} is 2: $R_{c1}/R_{c2} = 2$. $R_1 = 2.6$ KΩ.

a). Calculate the output voltage, V_o, and prove that it is possible to have a voltage reference.

b). Calculate the value of the curents I_{c1} and I_{c2}.

You have: ln2 = 0.693 ; ln5 = 1.6 ; ln10=2.3 ; V_T= 26mV at 300 K.



ANSWERS:

1. At the left-hand side of the figure, the first block is a differential input stage with emitter followers (Ql and Q2) driving common-base stages (Q3 and Q4).

The transistors Q5 and Q6 form an active load for Q3 and Q4.

Q7, Q5, Q6 and their emitter resistances form a simple current mirror with degeneration.

The two pairs of transistors shown at the top of the schematic are simple current mirrors (Q8 and Q9, Q12 and Q13).

At the bottom is a Widlar current source (built by Q10, Q11, and the 5 kΩ resistor).

Transistors Q15, Q19 and Q22 function as a class A gain stage. The stage consists of two NPN transistors in a Darlington configuration (Q15 and Q19).

Transistor Q16 and its base resistors is the V_{be} multiplier voltage source.

Transistors Q14, Q20 form the class AB push-pull emitter follower output stage.

Answer (AIC problem 2)

We consider an ideal op amp.

$\Rightarrow V_{Rc_1} = V_{Rc_2} \Leftrightarrow I_{c_1} R_{c_1} = I_{c_2} R_{c_2} \Rightarrow \frac{I_{c_2}}{I_{c_1}} = \frac{R_{c_1}}{R_{c_2}} = 2$ (1)

KVL in the loop of R_1 and two V_{BE}:

$V_{BE_2} + I_{c_1} R_1 = V_{BE_2} \Leftrightarrow I_{c_1} R_1 = V_{BE_2} - V_{BE_1} =$

$= V_T \ln \frac{I_{c_2}}{I_{S_2}} - V_T \ln \frac{I_{c_1}}{I_{S_1}}$

But T_1 and T_2 are identical $\Rightarrow I_{S_1} = I_{S_2}$

$\Rightarrow I_{c_1} R_1 = V_T \ln \frac{I_{c_2}}{I_{c_1}} = V_T \ln 2$

$\Rightarrow I_{c_1} = \frac{V_T \ln 2}{R_1}$ (2)

$V_{out} = V_{BE_2} + V_{R_1} = V_{BE_2} + (I_{c_1} + I_{c_2}) R_2$ (3)

$\overset{(3),(1)}{\Longrightarrow} V_{out} = V_{BE_2} + (I_{c_1} + 2 I_{c_1}) R_2 \overset{(2)}{=} V_{BE_2} +$

$+ 3 \cdot R_2 \cdot \frac{V_T \ln 2}{R_1} = V_{BE_2} + \left(3 \cdot \frac{R_2}{R_1} \cdot \ln 2\right) \cdot V_T$

V_{out} will be compensated if:

$3 \frac{R_2}{R_1} \ln 2 = N = 23 \Rightarrow R_2 = \frac{23 \cdot R_1}{3 \cdot \ln 2}$

$\Rightarrow R_2 = \frac{23 \cdot 2{,}6 \cdot 10^3}{3 \cdot 0{,}693} \cong 28{,}7\ K\Omega.$

So, if $R_2 = 28{,}7\ K\Omega$ we have a band-gap referenced circuit and the output voltage is: $V_{out} = V_{BE} + N \cdot V_T \cong 0{,}6V + 23 \cdot 26mV \cong 1{,}2V$

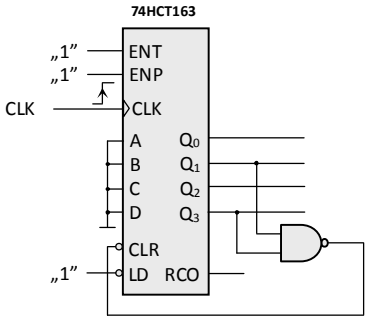
b). $I_{c_1} = \frac{V_T \ln 2}{R_1} = \frac{26 \cdot 10^{-3} \cdot 0{,}693}{2{,}6 \cdot 10^3} \cong 0{,}7\mu A$

$I_{c_2} = 2 \cdot I_{c_1} = 14\mu A$

Digital Integrated Circuits

1. Use a 74x163 binary synchronous counter (synchronous reset) to design a modulus 11 counter (the counting sequence is: 0, 1, 2, ..., 10, 0, 1, 2, ...). Explain what happens if reset is asyncronous.

Solution:. A nAND gate is used to detect the 10 state ($Q_3Q_2Q_1Q_0$ = 1010) and by clearing the counter the next state will be 0000. A different modulus is obtained if the reste is asyncronous.



2. Using EPROM 27C256 memories (32k x 8 bits) and glue logic, design a 64k x 8 bits memory.

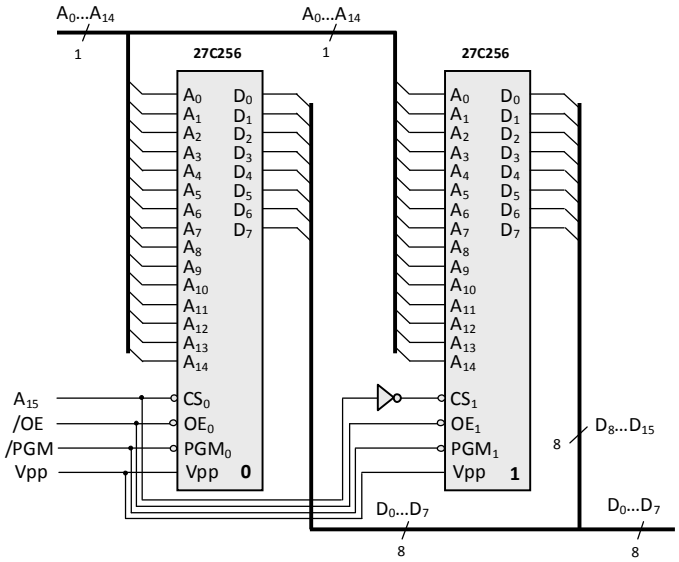
Solution: a). The needed number of EPROM circuits is:

$$N = \frac{64k\,x8}{32k\,x8} = 2\,.$$

b). The initial memory has 15 address lines (A_0, ..., A_{14}). The final memory has 16 address lines.

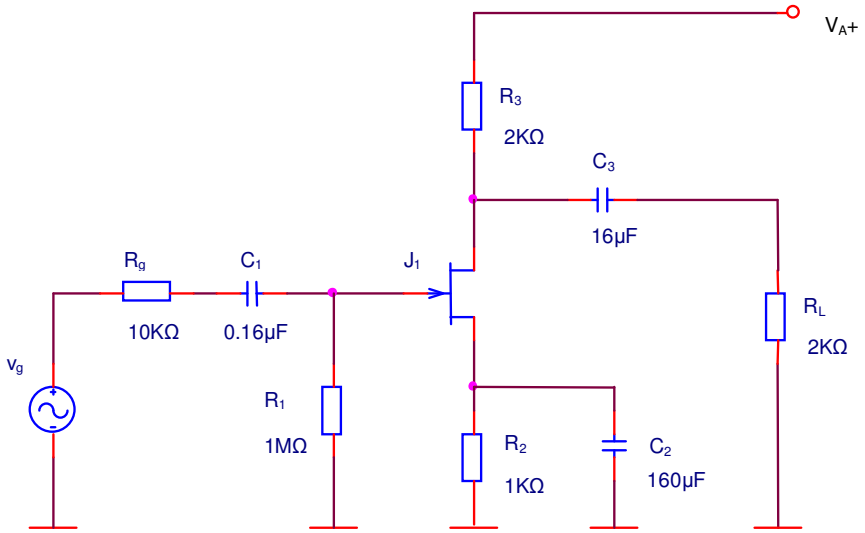
A_{15}	$A_{14} - A_0$	Memory #	Enable	
			$\overline{CS_0}$	$\overline{CS_1}$
0	X..... X	0	0	1
1	X..... X	1	1	0

The final schematic is:



Electronic Circuits

1. For the circuit below, having the J-FET with parameters: $g_m = 5\text{mA/V}$, $r_{ds} = \infty$, $C_{gd} = 5\text{pF}$, $C_{gs} = 10\text{pF}$, $C_{ds} = 10\text{pF}$.
   Find out the high cutt off frequency by:
   a) Using Miller Theorem;
   b) Using OCTC (Open Circuit Time Constant) method.



Solution: Seminar nr 2.pdf pag. 3,4

Se desenează schema echivalentă la frecvențe înalte și semnal mic (fig. 9).

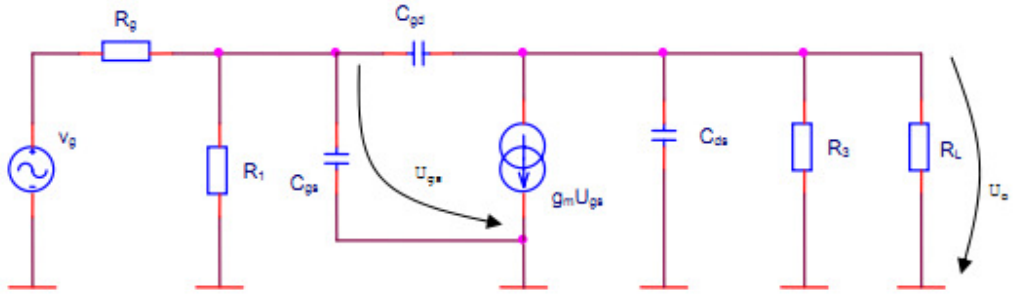


Fig. 9. Schema echivalentă la frecvențe înalte și semnal mic pentru circuitul din fig. 8.

a) Folosind teorema lui Miller se elimină capacitatea C_{gd} rezultând schema echivalentă din fig. 10.

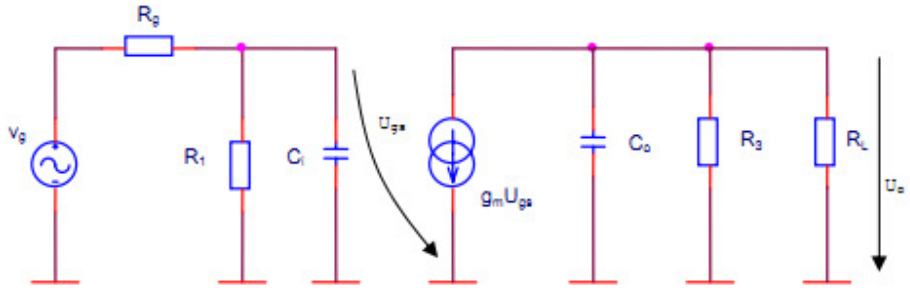


Fig. 10. Schema echivalentă după aplicarea teoremei lui Miller.

$K = \frac{U_o}{U_i}$ şi $U_o = - g_m U_{gs} (R_3 || R_L)$, $U_i = U_{gs} \Rightarrow$ K = $A_{U0} = - g_{ms} R_3 || R_L = -5$

$C_{iM} = C_{gd}(1-K) = 30$ pF, $C_{oM} = C_{gd}\left(1 - \frac{1}{K}\right) = 6$ pF

$C_i = C_{gs} || C_{iM} = C_{gs} + C_{iM} = 40$ pF, $C_o = C_{ds} || C_{oM} = C_{ds} + C_{oM} = 16$ pF

Frecvențele introduse de aceste capacități sunt:

$$f_{P1} = \frac{1}{2 \cdot \pi \cdot C_i \cdot R_{P1}}, R_{P1} = R_g \| R_1 \cong R_g \cong 10K\Omega \Rightarrow f_{P1} = 400KHz$$

$$f_{P2} = \frac{1}{2 \cdot \pi \cdot C_o \cdot R_{P2}}, \; R_{P2} = R_3 \| R_L = 1K\Omega \Rightarrow f_{P2} = 10MHz \, .$$

Funcția de transfer la înaltă frecvență va fi atunci:

$$A_U(j\omega) = -5 \cdot \frac{1}{(1 + j\frac{f}{0.4 \cdot 10^6}) \cdot (1 + j\frac{f}{10 \cdot 10^6})}$$

Relația de mai sus este aproximativă deoarece condensatorul C_{gd} introduce și o frecvență de zero.

Frecvența de trecere la înalte se poate apoxima prin f_{P1} = 400KHz sau se poate calcula pe baza definiției:

$$\left|A_U(j\omega)\right|_{f=f_i} = \frac{1}{\sqrt{2}} A_{U0} \Rightarrow f_i = 393{,}7\text{KHz} \tag{27}$$

b) Metoda se aplică, relativ la schema echivalentă la frecvențe înalte, prezentată fig. 9. Se analizează pe rând efectul fiecărei capacități:

b1) Analiza efectului capacității C_{gs}.

Schema echivalentă obținută prin aplicarea metodei constantelor de gol este cea din fig. 11.

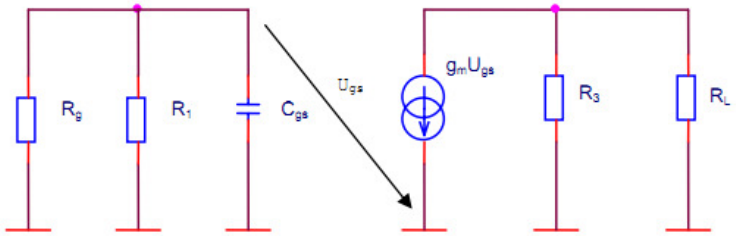


Fig. 11. Schema echivalentă, cazul C_{gs}.

$$f_{P1} = \frac{1}{2 \cdot \pi \cdot C_{gs} \cdot R_{P1}}, R_{P1} = R_1 \| R_g \cong R_g \cong 10K \Rightarrow f_{P1} = 1{,}6MHz \tag{28}$$

b2) Analiza efectului capacității C_{gd}.

Schema echivalentă obținută prin aplicarea metodei constantelor de gol este prezentată în fig. 12.

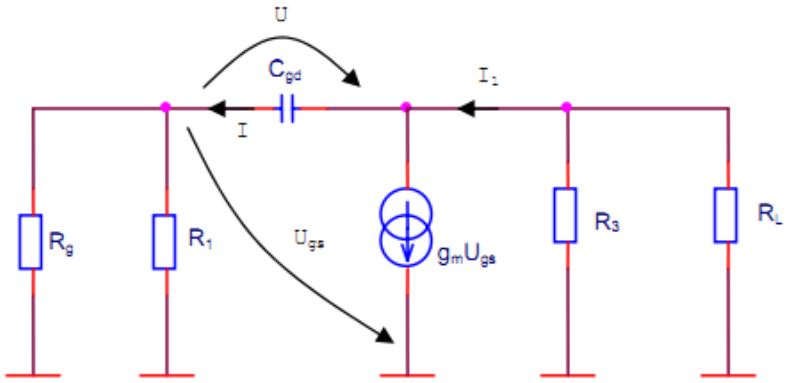


Fig. 12. Schema echivalentă, cazul C_{gd}.

$$f_{P2} = \frac{1}{2 \cdot \pi \cdot C_{gd} \cdot R_{P2}}, R_{P2} = \left|\frac{U}{I}\right|$$

Aplicând teoremele lui Kirchhoff se pot scrie următoarele relații:

$$-i \cdot R_g \| R_1 + u_{gs} = 0 \Rightarrow u_{gs} = i \cdot R_g \| R_1$$

$$I_1 = g_m \cdot u_{gs} + I = I(1 + g_m \cdot R_g \| R_1)$$

$$U - I \cdot R_g \| R_1 - I_1 \cdot R_3 \| R_L = 0 \Rightarrow U = I \cdot R_g \| R_1 + I \cdot (1 + g_m \cdot R_g \| R_1) \cdot R_3 \| R_L$$

$$R_{P2} = \frac{U}{I} = R_g \| R_1 + (1 + g_m \cdot R_g \| R_1) \cdot R_3 \| R_L = 61\text{K}\Omega. \Rightarrow f_{P2} = 524{,}6KHz$$

b3) Analiza efectului capacității C_{ds}

Schema echivalentă obținută prin aplicarea metodei constantelor de gol este cea din fig. 13.

$$f_{P3} = \frac{1}{2 \cdot \pi \cdot C_{ds} \cdot R_{P3}},\ R_{P3} = R_3 \| R_L = 1K \Rightarrow f_{P3} = 16MHz$$

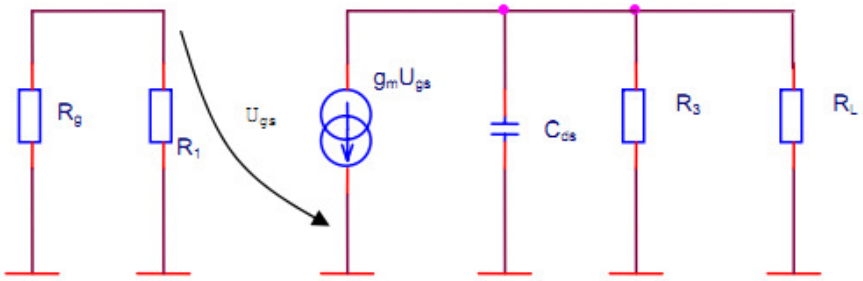


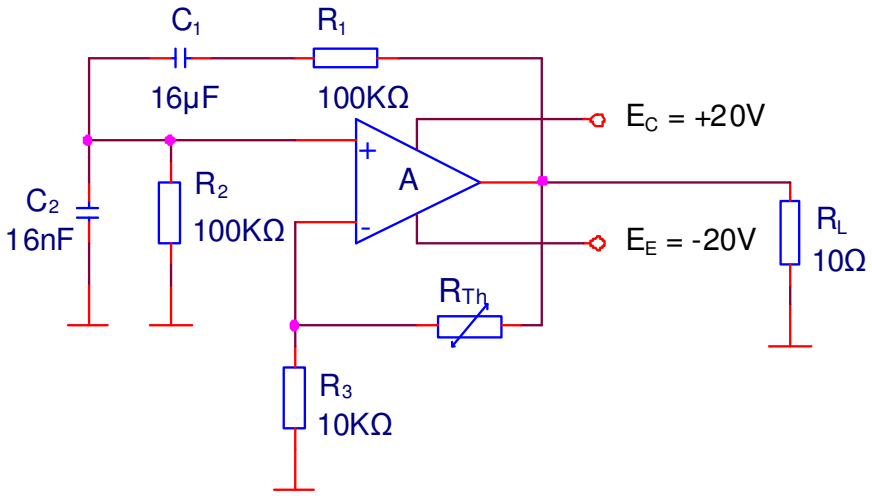
Fig. 13. Schema echivalentă, cazul C_{ds}.

Efectul cumulat al celor trei capacități se determină astfel:

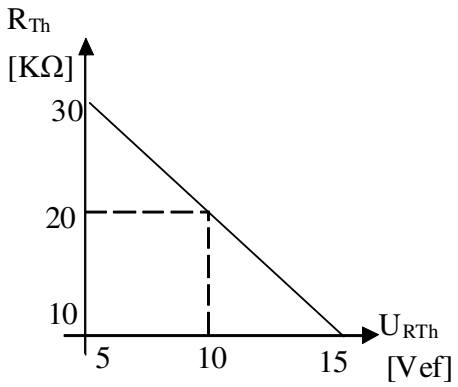
$$\frac{1}{f_i} = \frac{1}{f_{i1}} + \frac{1}{f_{i2}} + \frac{1}{f_{i3}} \Rightarrow f_i \cong 385{,}2KHz.$$

2. The schematic below is a Wien oscillator using a class B final stage amplifier having: $A_u \to \infty$, $R_i \to \infty$, $R_o \to 0$. Find out:

a) f_o oscillating frequency,
b) V_0, when using the thermistor R_{Th};
c) P_0 (delivered to R_L)



Solution: 2010 Sem 7.ppt pag. 4,5.



Solution

a) $f_o = \frac{1}{2 \cdot \pi \cdot \sqrt{R_1 R_2 C_1 C_2}} \cong 100Hz$

b) A = 1 + R_{Th}/R_3 , and at f_0: |β| = 1/3.

From |A||β| = 1 => R_{Th} = 20KΩ obtained for U_{Th} = 10V
Because feedback is a voltage divider including R_{Th} :

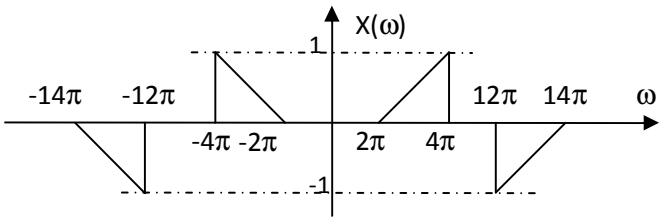
$$u_{Rth} = u_o \cdot \frac{R_{Th}}{R_{Th} + R_3} = \frac{2}{3} \cdot u_o \Rightarrow u_o = 1{,}5 \cdot u_{Rth} = 15V_{ef}$$

$$u_{om} = \sqrt{2} \cdot 15V_{vv}$$

c) $P_o = \frac{u_{om}^{\ 2}}{2 \cdot R_L} = 22{,}5W$

Signal Processing

1- Consider the signal $x(t)$ with the spectrum below



What is the minimum sampling frequency $f_{s\min}$ according to the sampling theorem?

A.

$$f_{s\min} = 2f_M = 2 \bullet 7Hz = 14Hz$$

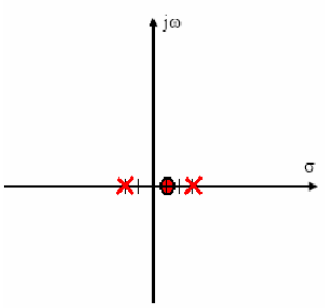
$$f_M = \frac{14\pi rad/s}{2\pi rad} = 7Hz$$

2 - Consider the system with the transfer function: $H(s) = \frac{s-1}{(s+2)(s-3)}$.

Sketch its pole/zero plot.

A.

$$X(s) = \frac{s-1}{(s+2)(s-3)}$$



x- pole
o - zero

Electronic Instrumentation

1. Determine the rise time of a 20MHz oscilloscope.

$$t_r(\text{ns}) = \frac{350}{B(\text{MHz})}$$

t_r=350/20 =17 ns.

2. Specify the measurement result for a 100% confidence level (result ± uncertainty, confidence level) according to the rules for data presentation when measuring a voltage of 12.45 V with a 3 ½ digit 20 V voltmeter whose maximum permissible error is given by

$$\Delta_t = 0{,}1\% \times \text{reading} + 0{,}05\% \times \text{range} + 1 \text{ digit}$$

Answer:

Solution. The DVM reads xx,xx V. Therefore,
1 digit = 10 mV.
The maximum permissible error when measuring 12.45 V is
$\Delta t = 0{,}1\% \times 12.45\ \text{V} + 0{,}05\% \times 20\ \text{V} + 10\ \text{mV}$,
or
$\Delta t = 32.45\ \text{mV} \cong 30\ \text{mV}$.
For a confidence level of 100%, the measurement result should be specified as
$U = 12.45\ \text{V} \pm 30\ \text{mV}$.