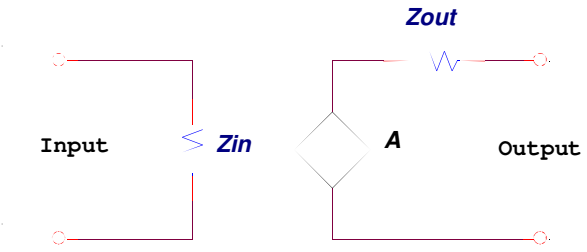
Electronic Circuits

1. Demonstrate the optimum input and output impedance for a voltage amplifier.
   2010 EC (c 01).ppt / slides 8,9

Amplifiers fundamental properties

- *Gain*
- *Input impedance*
- *Output impedance*



General amplifier model

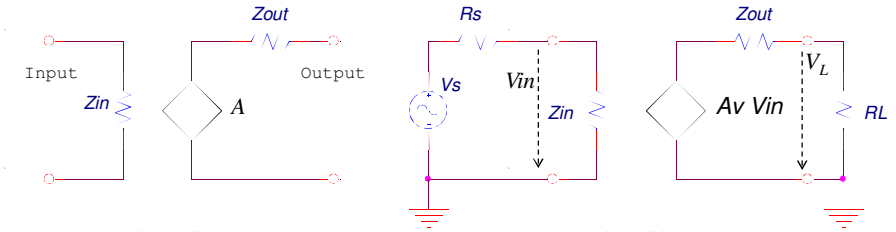
- There are three types of gain:

voltage gain (A_V),
current gain (A_I),
power gain (A_P).

$$A_v = \frac{V_{out}}{V_{in}} \quad A_i = \frac{i_{out}}{i_{in}} \quad A_p = \frac{p_{out}}{P_{in}}$$

- The gain of a circuit is determined by its component values !!!
- When the gain of a circuit has been calculated, it can be used to determine the output from the circuit for a specified input

Ex: Voltage amplifier circuit



Amplifier model *Amplifier circuit*

- At the circuit input and output there are 2 voltage dividers:

$$V_{in} = V_S \frac{Z_{in}}{R_S + Z_{in}} \quad V_L = V_{out} \frac{R_L}{Z_{out} + R_L}$$

where $v_{out} = A_V v_{in}$

- Since $v_{in} < v_S$ and $v_L < v_{out}$,

=> The *effective voltage gain* of a circuit is lower than the calculated voltage gain of the amplifier itself.

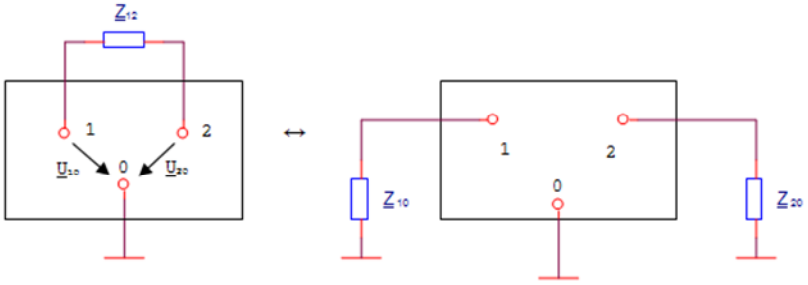
To neglect the input and output voltage drop we must have :

***[Infinite gain], Infinite input impedance, Zero output impedance* !!!**

2. Explain Miller effect and theorem and its utility for high frequency analysis.
2010 EC (c 03+04).ppt /slides 37-38, seminar nr.2.doc

Miller Effect

An impedance Z_{12} connected from the input of an amplifier to the output can be replaced by an impedance across the input terminals (Z_{10}) and impedance across the output terminals (Z_{20}).



Miller theorem:

$$\begin{cases} \underline{Z}_{10} = \underline{Z}_{12} \cdot \dfrac{1}{1-K} \\ \underline{Z}_{20} = \underline{Z}_{12} \cdot \dfrac{1}{1-\dfrac{1}{K}} \end{cases}$$

where: $K = \dfrac{\underline{U}_{20}}{\underline{U}_{10}}$ (voltage gain computed at midband frequency !)

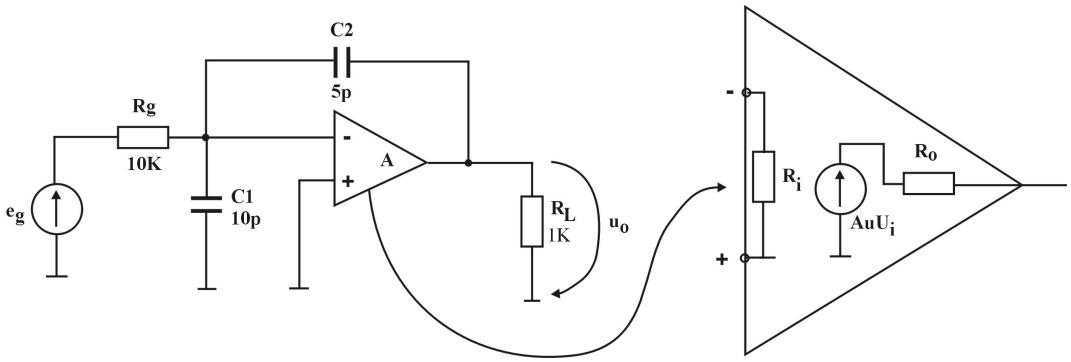
For a capacitor:

$$\begin{cases} C_{10} = C_{12}(1-K) \\ C_{20} = C_{12}\left(1-\dfrac{1}{K}\right) \end{cases}$$

It could be used in high-frequency circuit analysis in order to eliminate feedback capacitances, admitting that K is computed at midband frequency, thus ignoring the zeros form the complex transfer function.

Example: For the following circuit, we consider the amplifier's parameters:

$A_u = 10^2; R_i = 1M\Omega; R_o = 1K\Omega$. Compute the upper limit frequency of the circuit, using Miller's theorem



Answer:

$$f_{p_1} = \frac{1}{2\pi(C_{10} + C_1)R_g \| R_i} = 60KHz, f_{p_2} = \frac{1}{2\pi(C_{20})R_g \| R_i} = 64KHz$$

$$C_{10} = C_2(1-K),\ C_{20} = C_2(1-\frac{1}{K}),\ K = \frac{U_o}{U_i} = \frac{A_u U_i \frac{R_L}{R_o + R_L}}{U_i} = A_u \frac{R_L}{R_o + R_L}$$

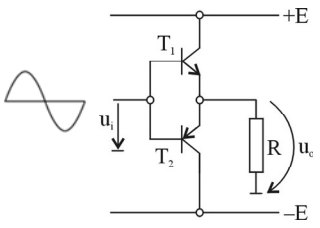
3. Which amplifier class is known for its crossover distortions? Explain the root cause and ways of improvement based on a simplified schematic and is transfer characteristic.

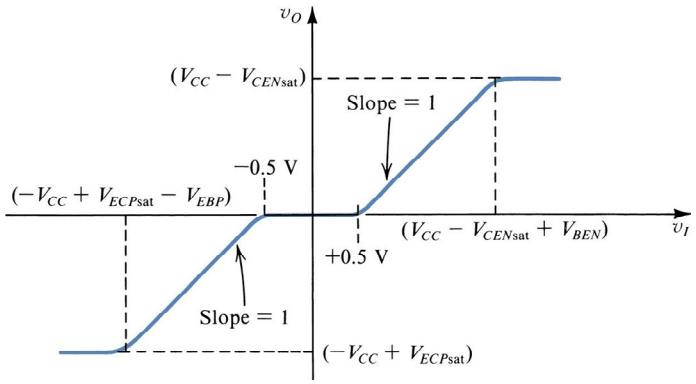
2010 EC (c 05).ppt / slides 22-24, 37

Class B - output stage circuit

Named also *Complementary-symmetry amplifier*

= 2 complementary BJT's used as emitter followers, working in "push pull" mode.

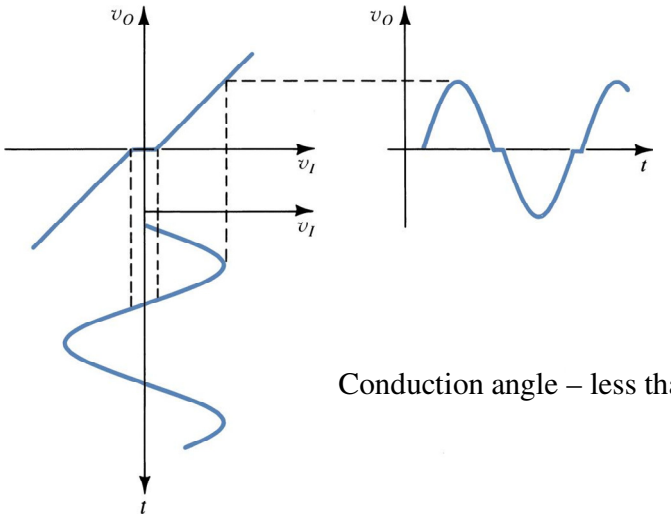




Advantage: good efficiency – up to 78.5% (in DC mode – no current sink from supply)

Drawback: Crossover distortion

Class B – crossover distortion

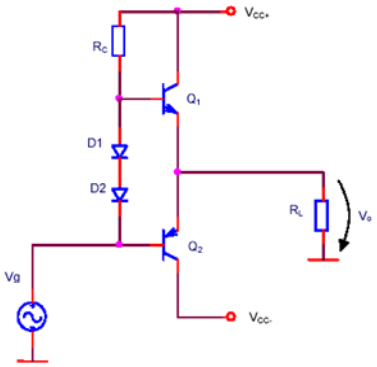


Conduction angle – less than ½ T

=> crossover distortion between the "halves" of the signal

Class B biasing

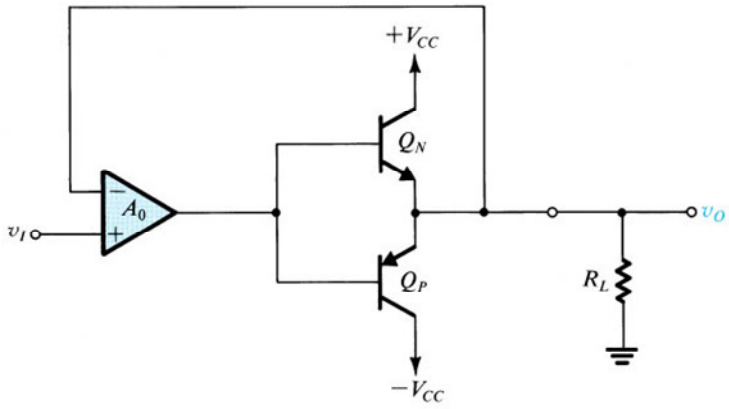
Biasing must provide V(B1)- V(B2) to keep Q1 and Q2 off, but close to conduction => lower crossover distortion



BJT 's can be biased using 2 diodes or a "V_{BE} multiplier" circuit => constant voltage drop between Q1 and Q2 bases

Opamp Implementation

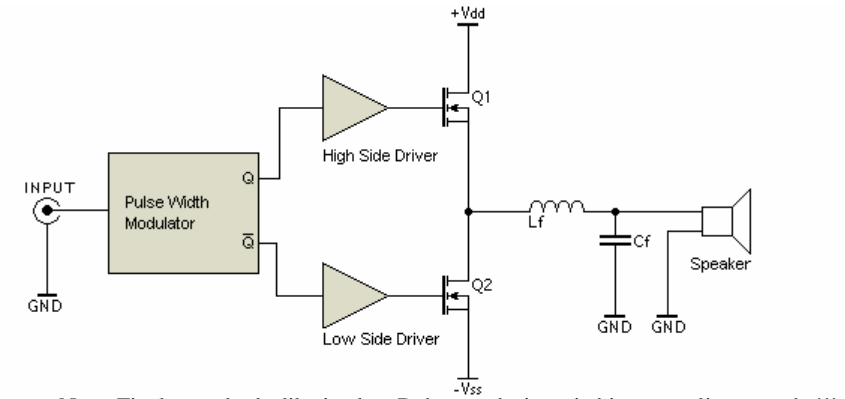
Op amp connected in a negative-feedback loop to reduce crossover distortion



4. Describe half bridge class D amplifiers topology, block schematic and principle of operation. 2010 EC (c 06).ppt / slides 5-7

Class D – (half bridge) simplified circuit

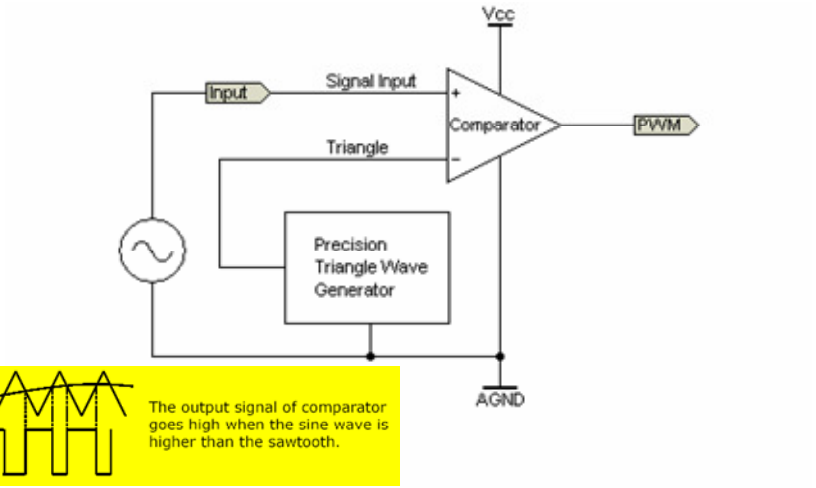
– operation is switching, hence the term *switching power amplifier*
– output devices are rapidly switched on and off at least twice for each cycle
– the output devices are either completely on or completely off so theoretically they do not dissipate any power



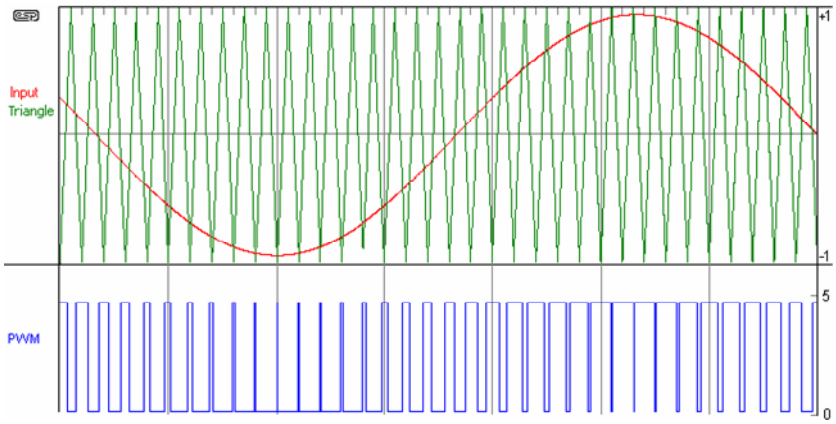
Note: Final stage looks like in class B, but works in switching – not linear mode !!!

Class D - PWM signal generation

▪The input signal is compared with a triangle signal resulting in a PWM (Pulse width modulation) signal



Class D – PWM waveforms

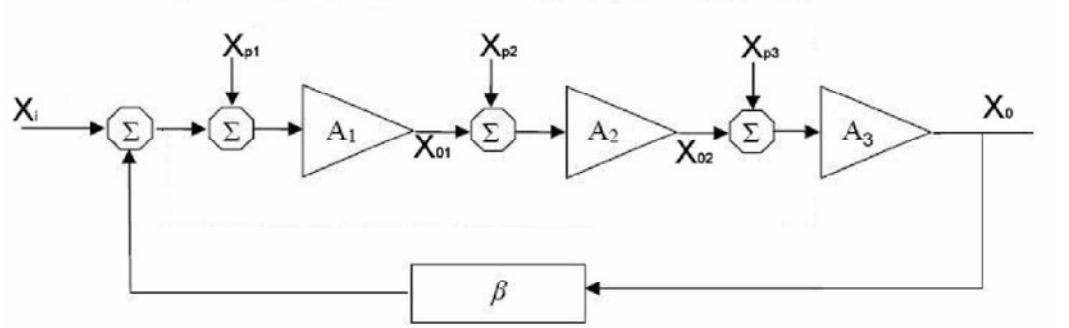


- Usually 150KHz to 250Khz switching freq. is used
- The LC LPF provide at the output the mean value of the PWM signal - same shape as the Input signal

5. Using formula show the most unwanted occurrence place for an external perturbation in a multistage amplifier sing a gobal negative feedback loop

2010 EC (c 07).ppt/ slide 11

Perturbation influence in Feedback Amps



$$\begin{cases} x_0 = (x_{02} + x_{p3})A_3 \\ x_{02} = (x_{01} + x_{p2})A_2 \\ x_0 = (x_\Sigma + x_{p1})A_1 \\ x_\Sigma = x_i - x_r = x_i - \beta x_0 \end{cases}$$

Perturbations are reduced as they are closer to output

$$x_0 = (((x_i - \beta x_0 + x_{p1})A_1 + x_{p2})A_2 + x_{p3})A_3$$

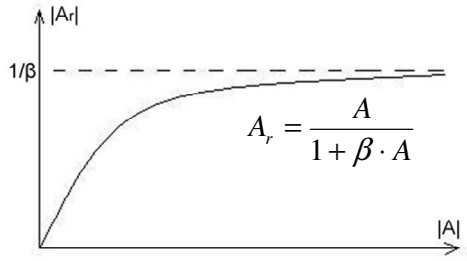
$$\Rightarrow x_0 = x_i \frac{A_1A_2A_3}{1+\beta A_1A_2A_3} + x_{p1}\frac{A_1A_2A_3}{1+\beta A_1A_2A_3} + x_{p2}\frac{A_2A_3}{1+\beta A_1A_2A_3} + x_{p3}\frac{A_3}{1+\beta A_1A_2A_3}$$

6. Demonstrate bandwidth extension for an amplifier when a negative feedback is applied.

2010 EC (c 07).ppt /slides 5-7

Feedback effect over gain

- For amplifiers with feedback we can assume that the



If nonfeedback amplifier has : $\Delta A / A$

$\Delta A_r / A_r$??? $\Delta A / A$

At small variations :

$$\Delta A_r \cong \frac{1+\beta A - A\beta}{(1+\beta A)^2} \cdot \Delta A = \frac{1}{(1+\beta A)^2} \cdot \Delta A = \frac{A}{1+\beta A} \cdot \frac{1}{1+\beta A} \cdot \frac{\Delta A}{A} \Rightarrow$$

$$\frac{\Delta A_r}{A_r} \cong \frac{\Delta A}{A} \cdot \frac{1}{1+\beta A} = \frac{\Delta A}{A} \cdot \frac{1}{F}$$

F times improvement !!!

Influence of the feedback on freq. response

If $A(j\omega) = \frac{P(j\omega)}{Q(j\omega)} \cdot A_0$ and $\beta = \beta_0$ a real number,

Then: $A_r(j\omega) = \frac{\frac{P}{Q} \cdot A_0}{1 + \beta_0 \frac{P}{Q} \cdot A_0} = \frac{PA_0}{Q + \beta_0 P A_0}$

only the poles are shifted

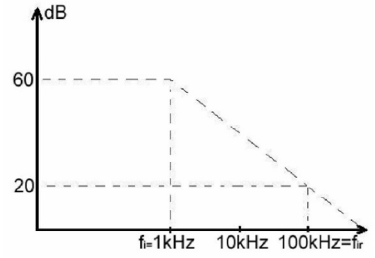
Influence of the feedback on freq. response(@high freq.)

$$\text{EX 1}: A(j\omega) = \frac{A_0}{1 + j\frac{f}{f_i}} \qquad \beta = \beta_0$$

$$A_r(j\omega) = \frac{\frac{A_0}{1 + j\frac{f}{f_i}}}{1 + \frac{\beta_0 A_0}{1 + j\frac{f}{f_i}}} = \frac{A_0}{1 + \beta_0 A_0 + j\frac{f}{f_i}} = \frac{A_0}{1 + \beta_0 A_0} \cdot \frac{1}{1 + j\frac{f}{f_i(1 + \beta_0 A_0)}} = A_{ro} \cdot \frac{1}{1 + j\frac{f}{f_{ir}}}$$

where $A_{r0} = \frac{A_0}{1 + \beta_0 A_0}$ & $f_{ir} = f_i(1 + \beta_0 A_0)$

Then: $A_r = \frac{A}{F}$; $f_{ir} = f_i F$; $A_r \cdot f_{ir} = A \cdot f_i$



Note: only if circuit still behave linear !!!

7. Show input and output resistance change for an amplifier when a shunt-shunt feedback is applied. Justify with formulas.

2010 EC (c 08).ppt / slides 7, 10

Shunt Shunt Negative Feedback

$$Z_{tA} = Z_{tr}\,|_{\,=0}$$

$$u_0 = Z_{tA} \cdot i_{iA} = Z_{tA}(i_g - i_r) = Z_{tA}(i_g - \beta u_0)$$

$$\Rightarrow \quad Z_{tr} = \frac{u_0}{i_g} = \frac{Z_{tA}}{1 + \beta \cdot Z_{tA}}$$

$$R_{ir} = \frac{u_i}{i_g}$$

$$i_g = i_r + i_{iA} = \beta u_0 + \frac{u_i}{\underbrace{R_g \| R_{of} \| R_i}_{R_{iA}}} = \beta u_0 + \frac{u_i}{R_{iA}} = \beta \cdot Z_{tA} \cdot i_{iA} + \frac{u_i}{R_{iA}}$$

$$i_g = \beta \cdot Z_{tA} \cdot \frac{u_i}{R_{iA}} + \frac{u_i}{R_{iA}} \quad \Rightarrow \quad R_{ir} = \frac{u_i}{i_g} = \frac{R_{iA}}{1 + \beta \cdot Z_{tA}}$$

Small value, because ig split also to the feedback network.

Shunt Shunt Negative Feedback

The output resistance determination

$$\frac{i_0}{u_0} = \frac{1}{R_{if}} + \frac{1+\beta Z_t}{R_0} = \frac{R_0 + R_{if} + \beta Z_t \cdot R_{if}}{R_{if} \cdot R_0}$$

$$\frac{i_0}{u_0} = \frac{R_0 + R_{if}}{R_{if} \cdot R_0}\left(1 + \beta Z_t \frac{R_{if}}{R_{if} + R_0}\right) = 1 \Big| R_{oA} \cdot \left(1 + \beta \left(Z_{tA}\right)_\infty\right)$$

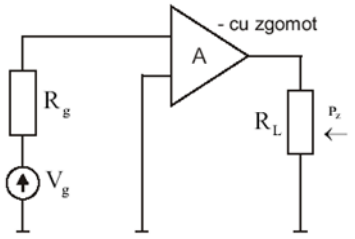
$$\left(Z_{tA}\right)_\infty = Z_{tA} \Big| R_L = \infty$$

$$R_{or} = \frac{R_{oA}}{1 + \beta \left(Z_{tA}\right)_\infty}$$

8. Draw noise equivalent schematic of an amplifier and define noise factor F.

2010 EC (c 11).ppt / slides 17, 18, 19

Noise model for an Amplifier

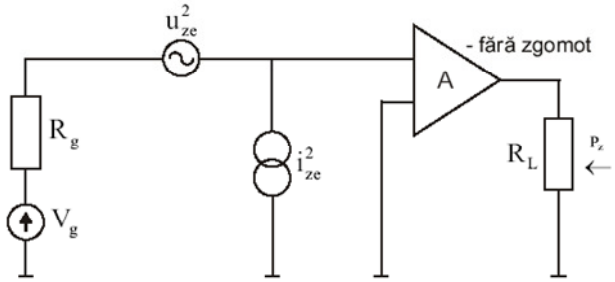


If the noise sources are uncorrelated, noise at output:

$$P_z = \sum_{k=1}^{n} P_{zk}$$

$$P_{zk} \rightarrow i_{zk}^2, u_{zk}^2 \rightarrow R_L$$

$u_{zet}^2 = u_{ze}^2 + i_{ze}^2 \cdot R_g^2$ Total noise voltage



Noise figure (factor)

- Compare noise produced by the amp. with the noise produced by the generator Rg

$$F = \frac{SNR_{in}}{SNR_{out}}$$ SNR – signal to noise ratio

$$F \overset{def}{=} \frac{\text{Puterea totală de zgomot de la iesire}}{\text{Puterea de zgomot datorată generatorului}}$$

$$F_{dB} = 10 \lg F$$

$$F_{dB} = 10 \lg \frac{P_{zg} + P_{zA}}{P_{zg}} \text{ unde } P_{zg} = \frac{u_{zg}^2}{(R_g + R_i)^2} \cdot R_i^2$$

$$P_{zA} = \frac{u_{ze}^2}{(R_g + R_i)^2} \cdot R_i^2 + \frac{i_{ze}^2 \cdot R_g^2}{(R_g + R_i)^2} \cdot R_i^2$$

$$F_{dB} = 10 \lg \left(1 + \frac{u_{ze}^2 + i_{ze}^2 \cdot R_g^2}{u_{zR_g}^2} \right) \qquad u_{zR_g}^2 = 4kTR_g \cdot \Delta f$$

Noise figure (factor)

- An optimum Rg exist for an given amplifier for which F=optimum:

$$F = F_{min} \qquad R_{g\,optim} = \sqrt{u_{ze}^2 / i_{ze}^2}$$

- For a CE BJT amplifier : $R_{g\,optim} \cong \frac{\sqrt{\beta}}{g_m}\sqrt{1 + 2g_m \cdot r_{bb'}}$

- For a FET amplifier $i_{ze} \cong 0 \qquad R_{g\,optim} \to \infty$

- If several stages are cascaded (Friis formula):

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \frac{F_4 - 1}{G_1 G_2 G_3} + \cdots + \frac{F_n - 1}{G_1 G_2 G_3 \cdots G_{n-1}},$$

9. Explain dominant pole (lag) compensation method. How is related dominant pole frequency to gain unity frequency f_{0dB}. Show practical implementation.

2010 EC (c 10) evo.ppt / slides 19-21

4.1 Dominant-pole compensation

It represents a very popular method, also called **lag compensation**. It consists in adding another pole in the open-loop transfer function - A(jω) - at a very low frequency, such that the loop-gain drops to unity by the time the phase reaches -180°:

$$A_C(j\omega) = A(j\omega)\frac{1}{1+j\dfrac{f}{f_d}}$$

$$f_d << \min(f_{pk})$$

where f_{pk} are the pole frequencies for A(jω).

A serious disadvantage of this compensation method is the resulting close-loop amplifier bandwidth, drastically reduced (fig. 4).

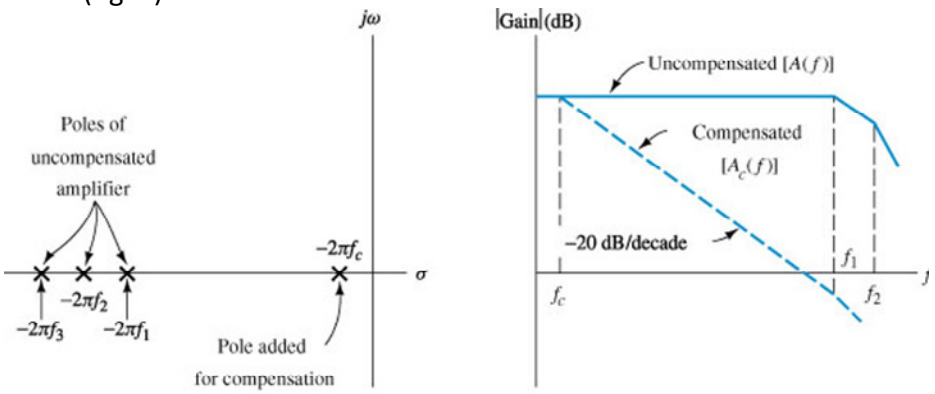


Fig. 4. Dominant-pole compensation.

It could be shown that knowing f_{0dB} is sufficient for computing f_d:

$$f_d = f_{0dB}\left|\frac{A_f}{A_0}\right|$$

where A_0 is the open-loop midband frequency gain.

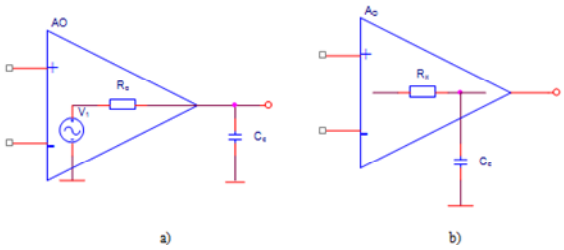


Fig. 5. Dominant-pole implementation.

10. Draw and characterize a Wien network and show how is connected to build a Wien oscillator. What are the conditions used to design feedback loops.

2010 EC (c 12,13).ppt / slides 17-19, 10
2010 Sem 7.ppt

3.2 The Wien Bridge Oscillator

An oscillator circuit in which a balanced bridge is used as the feedback network is the Wien bridge oscillator shown in fig. 4.

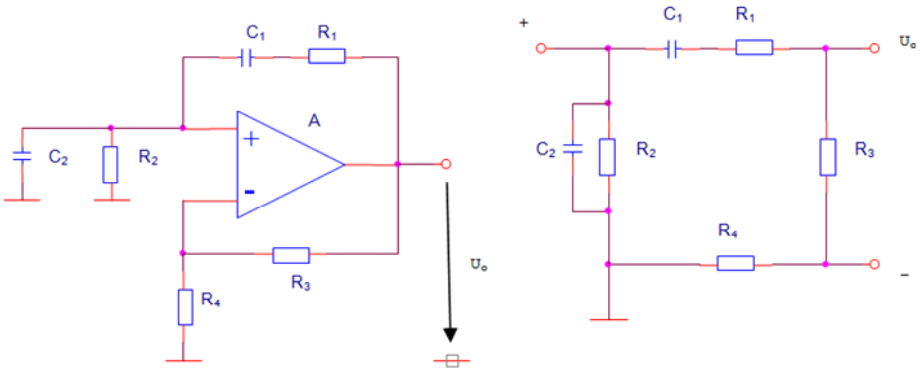


Fig. 4. a) A Wien bridge oscillator. b) The bridge network

$$\left|\underline{A}_{ur}\right|\left|\underline{\beta}_{+}\right|_{\omega=\omega_0}=1$$

$$\underline{A}_{ur}=\frac{A_u}{1+\beta_{-}A_u}\cong\frac{1}{\beta_{-}}$$

$$\left|\underline{\beta}_{+}\right|=\left|\underline{\beta}_{-}\right|$$

$$\beta_{-}=\frac{R_4}{R_3+R_4}$$

$$\beta_{+}(j\omega)=\frac{1}{1+\frac{R_1}{R_2}+\frac{C_2}{C_1}+j\left(\omega C_2R_1-\frac{1}{\omega C_1R_2}\right)}$$

In order to obtain oscillations:

$$\beta_{+}(j\omega_0)\in\Re\Rightarrow\omega_0C_2R_1-\frac{1}{\omega_0C_1R_2}=0;$$

$$\omega_0^2=\frac{1}{R_1C_1R_2C_2}\Rightarrow f_0=\frac{\omega_0}{2\pi}=\frac{1}{2\pi\sqrt{R_1C_1R_2C_2}}$$

$$\begin{cases}\arg\left[\beta_{+}(j\omega_0)\right]=0\\ \left|\beta_{+}(j\omega_0)\right|=\dfrac{1}{1+\dfrac{R_1}{R_2}+\dfrac{C_2}{C_1}}\end{cases}$$

Thus the condition for the feedback loop to provide sinusoidal oscillation of frequency ω is:

$$A(j\omega)\beta(j\omega)=1 \Leftrightarrow \begin{cases} \arg A(j\omega)+\arg \beta(j\omega)=2k\pi \\ \left|A(j\omega)\right|\left|\beta(j\omega)\right|=1 \end{cases}$$

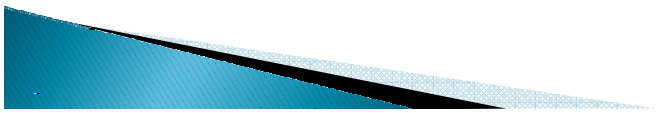
The above expressions taken together are called the **Barkhausen Criterion**.

The first relation is called **phase criterion** and the second **amplitude criterion**.

Digital Integrated Circuits

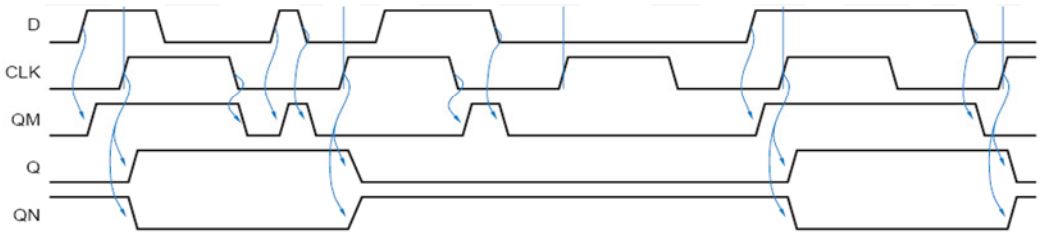
1. **Positive edge triggered D type flip-flop: draw a symbolic representation, the operating table and its associated waveforms**

    - Latches and Flip-Flops, slide 71-74



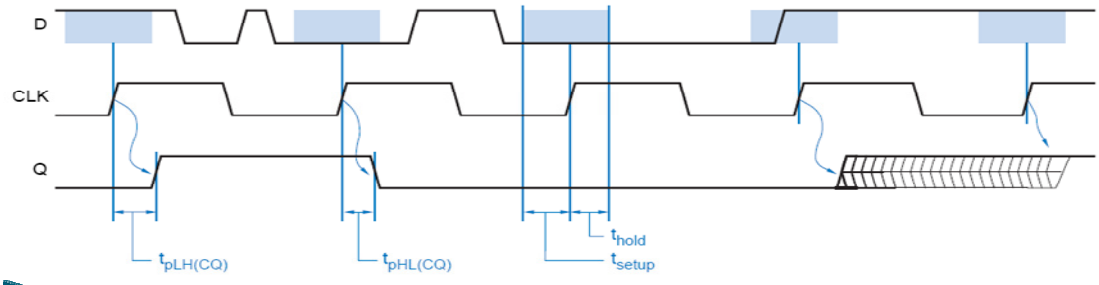
Edge-Triggered D Flip-Flop

- The QM signal shown is the output of the master latch.
- Notice that QM changes only when CLK is 0. When CLK goes to 1, the current value of QM is transferred to Q, and QM is prevented from changing until CLK goes to 0 again.



Edge-Triggered D Flip-Flop

- Like a D latch, the edge-triggered D flip-flop has a setup and hold time window during which the D inputs must not change.
- This window occurs around the triggering edge of CLK, and is indicated by shaded color.



2. Explain how a decoder can be used as a demultiplexer

- Combinational Circuits slide 16-20

The 74x138 3-to-8 Decoder

- The *74x138 is a commercially available MSI 3-to-8 decoder whose gate-level* circuit diagram and symbol are shown in Figure 5-37; its truth table is given in Table 5-7.
- Like the 74x139, the 74x138 has active-low outputs, and it has three enable inputs (G1, nG2A, nG2B), all of which must be asserted for the selected output to be asserted.
- Thus, we can easily write logic equations for an internal output signal such as Y5 in terms of the internal input signals:
- However, because of the inversion bubbles, we have the following relations between internal and external signals:
- Y5 = G1.G2A.G2B . C . nB . A
  Enable Select

- Therefore, if we're interested, we can write the following equation for the external output signal Y5_L in terms of external input signals:
  - G2A = nG2A_nL
  - G2B = nG2B_nL
  - Y5 = nY5_nL
- Y5_L = nY5 = n(G1 . nG2A_nL . nG2B_nL . C . nB . A)
- = nG1 + G2A_L + G2B_L + nC + B + nA

74x138 – Truth Table

Inputs						Outputs							
G1	nG2a	nG2b	C	B	A	nY7	nY6	nY5	nY4	nY3	nY2	nY1	nY0
0	x	x	x	x	x	1	1	1	1	1	1	1	1
x	1	x	x	x	x	1	1	1	1	1	1	1	1
x	x	1	x	x	x	1	1	1	1	1	1	1	1
1	0	0	0	0	0	1	1	1	1	1	1	1	0
1	0	0	0	0	1	1	1	1	1	1	1	0	1
1	0	0	0	1	0	1	1	1	1	1	0	1	1
1	0	0	0	1	1	1	1	1	1	0	1	1	1
1	0	0	1	0	0	1	1	1	0	1	1	1	1
1	0	0	1	0	1	1	1	0	1	1	1	1	1
1	0	0	1	1	0	1	0	1	1	1	1	1	1
1	0	0	1	1	1	0	1	1	1	1	1	1	1

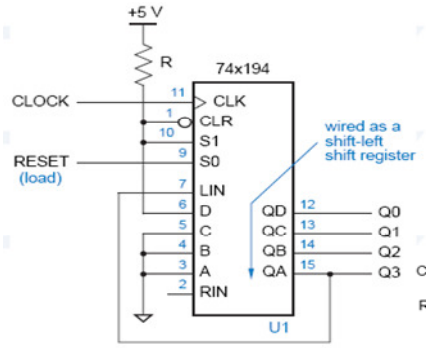
3. 4 bit Ring counter: schematic, explain its operation, main waveforms

- Registers, slide 75-80

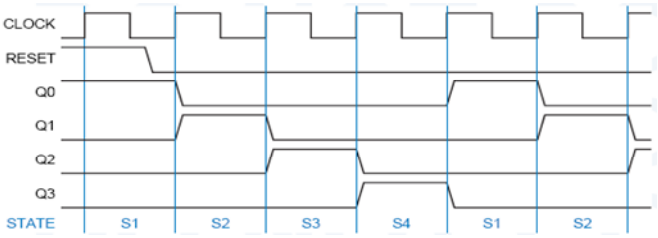
Ring Counters

- The simplest shift-register counter uses an n-bit shift register to obtain a counter with n states, and is called a *ring counter*.
- *Figure shows the logic diagram for a* 4-bit ring counter.
- The 74x194 universal shift register is wired so that it normally performs a left shift.
- However, when RESET is asserted, it loads 0001 (refer to the '194's function table).
- Once RESET is negated, the '194 shifts left on each clock tick. The LIN serial input is connected to the "leftmost" output, so the next states are 0010, 0100, 1000, 0001, 0010, ….
- Thus, the counter visits four unique states before repeating.
- A timing diagram is shown.
- An *n-bit ring counter visits n states in a cycle.*

Ring Counters

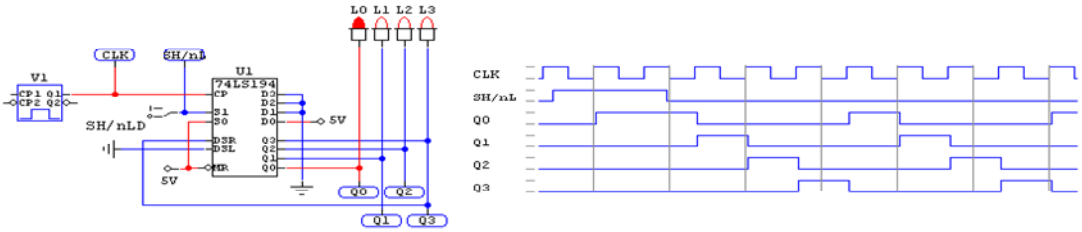


Simplest design for a four-bit, four-state ring counters with a single circulating 1.



Timing diagram for a 4-bit ring counter

Ring Counters



Ring counter with 74LS194 and timing diagrams.

Ring Counters

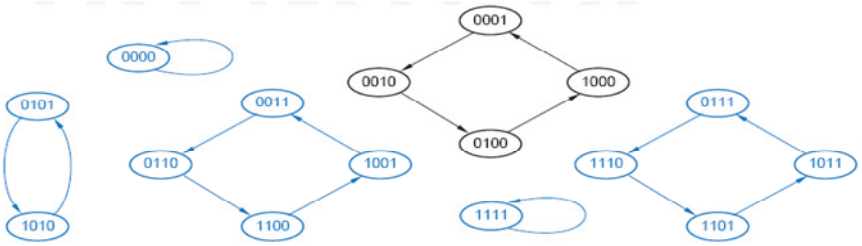
	CLK	Q_0	Q_1	Q_2	Q_3	Explicație
Initialiaze	0	0	0	0	0	nMR = 0
	1	1	0	0	0	S1 S0 = 11 (parallel load)
Complete cycle: 4 CLKs	2	0	1	0	0	S1 S0 = 01 (shift right)
	3	0	0	1	0	
	4	0	0	0	1	
	5 (1)	1	0	0	0	

Ring Counters

- The ring counter already introduced has one major problem—it is not robust.
- If its single 1 output is lost due to a temporary hardware problem (e.g., noise), the counter goes to state 0000 and stays there forever.
- Likewise, if an extra 1 output is set (i.e., state 0101 is created), the counter will go through an incorrect cycle of states and stay in that cycle forever.
- These problems are quite evident if we draw the *complete state diagram for the counter circuit, which has 16 states.*

Ring Counters

- As shown, there are 12 states that are not part of the normal counting cycle. If the counter somehow gets off the normal cycle, it stays off it.

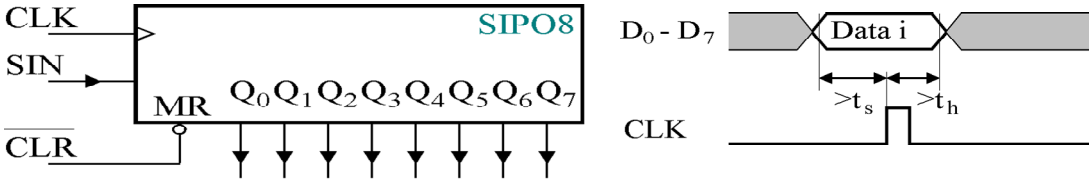


4. Describe how to achieve parallel-to-serial, respectively serial-to-parallel data conversion

- Registers 65 - 71

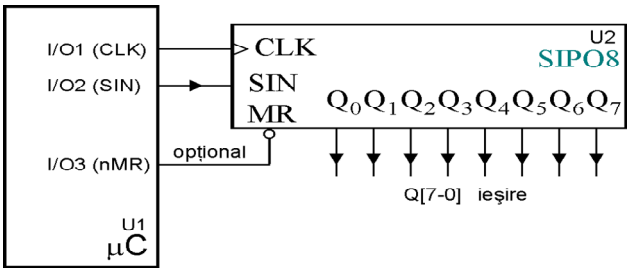
Serial – parallel conversion

- Uses a SIPO register:



Serial – parallel conversion

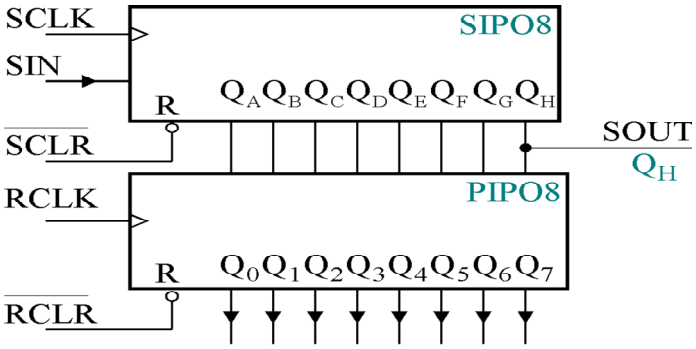
- Used for expanding the output pins for a low count pin microprocessor system
- E.g. PIC16F84A has 18 pini, 13 are I/O
- 2 pins are used and extra 8 outputs are provided



Expanding the output lines of a microcontroller

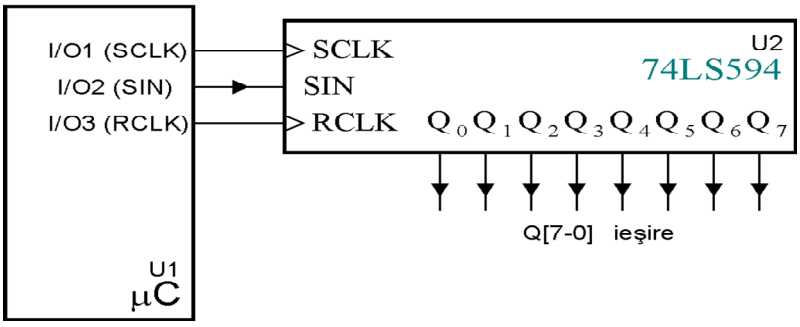
Serial – parallel conversion

- Problems when connecting fast devices
- Solution: 74LS594 register



74LS594 – functional diagram

Serial – parallel conversion

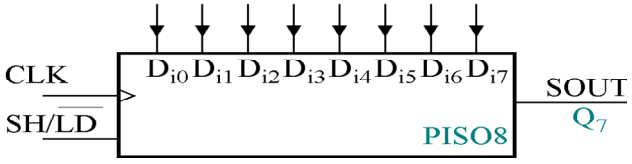


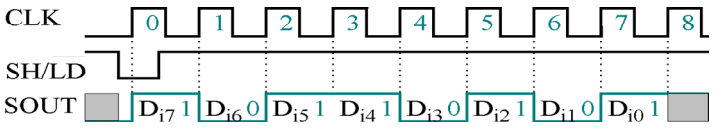
Expanding the Output lines of a microcontroller, 2nd version

Homework. How many I/O lines are necessary to control 16 output lines?

Parallel – serial conversion

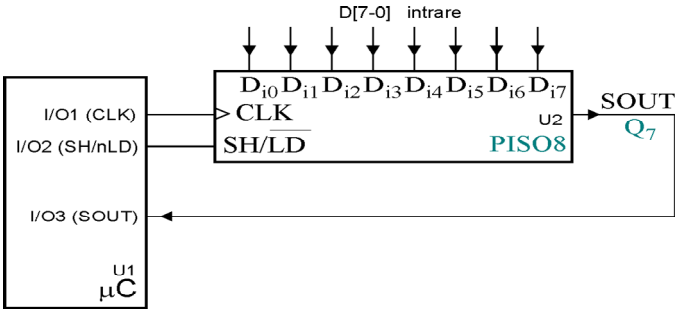
- Uses a PISO register:





Parallel – serial conversion

- Parallel – serial conversion can be used to expand the input lines in a microcontroller system

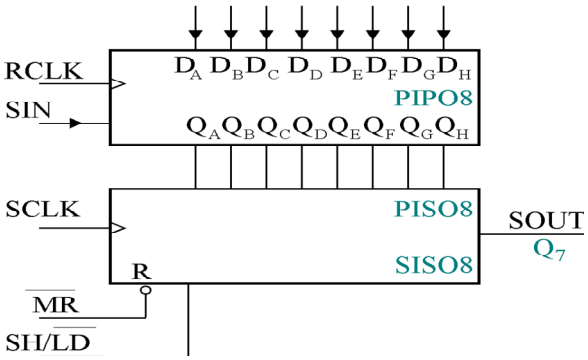


Expanding the input lines of a microcontroller

Parallel – serial conversion

- Same problem as before (with fast devices)
- Solution: 74LS597 register

Homework. How many I/O lines are necessary to control 16 input lines?



74LS597 – functional diagram

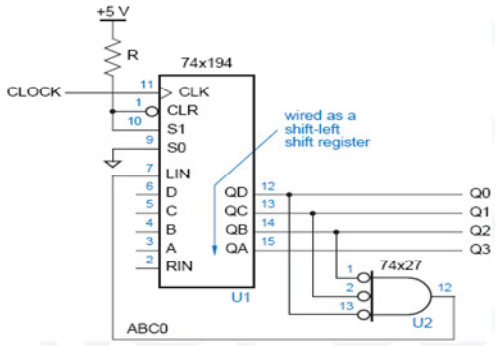
5. Self correcting counters built arround registers. Give at least 2 examples: schematic, explain its operation, main waveforms

- Registers slide 82 - 85.

Self Correcting Ring Counters

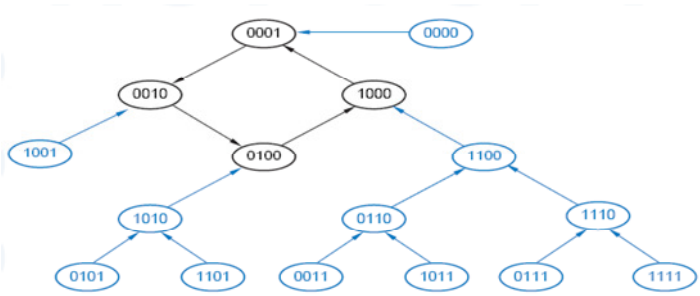
- A *self-correcting ring counter* circuit is shown. *The circuit* uses a NOR gate to shift a 1 into LIN only when the three least significant bits are 0.

No reset needed. Why?



Self correcting Counters

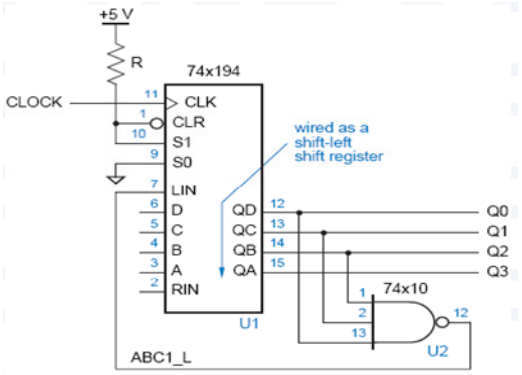
- This results in the state diagram; all abnormal states lead back into the normal cycle.



- For the general case, an *n-bit self-correcting ring counter uses an n-1-input* NOR gate, and corrects an abnormal state within *n - 1 clock ticks.*

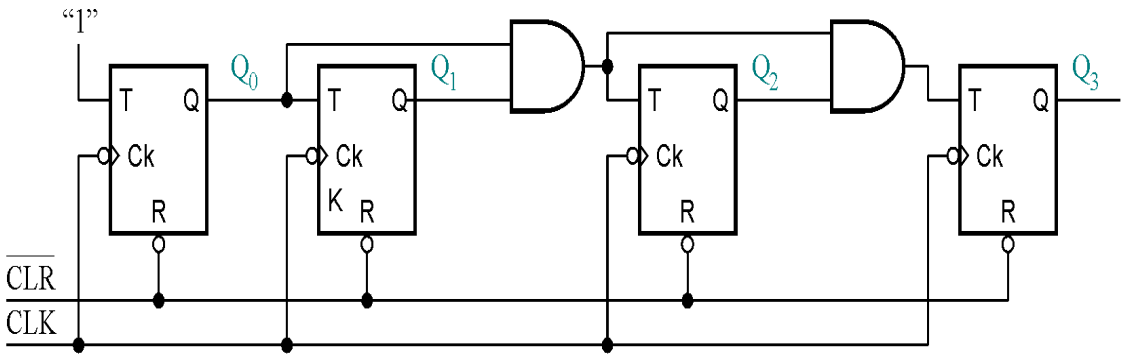
Self correcting Counters

- In CMOS and TTL logic families, wide NAND gates are generally easier to come by than NORs, so it may be more convenient to design a self-correcting ring counter as shown in Figure.
- States in this counter's normal cycle have a single circulating 0.

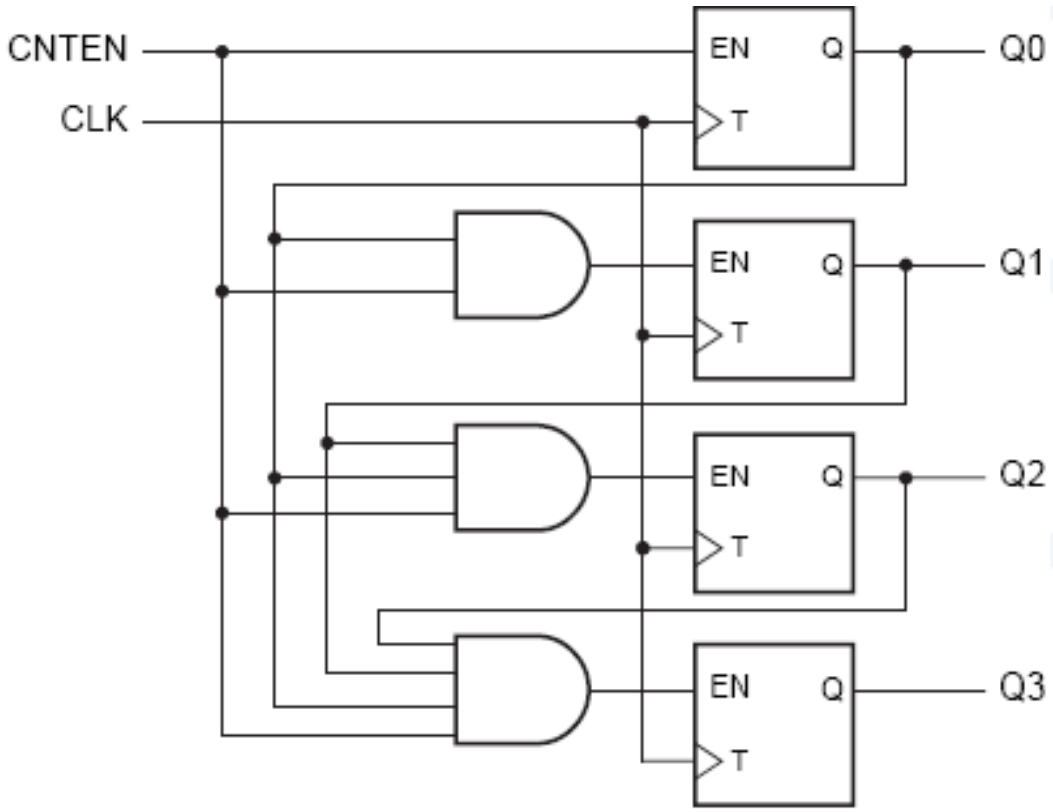


6. 4-bit binary synchronous counter. Draw the schematic diagram, explain its operation, and draw the relevant waveforms

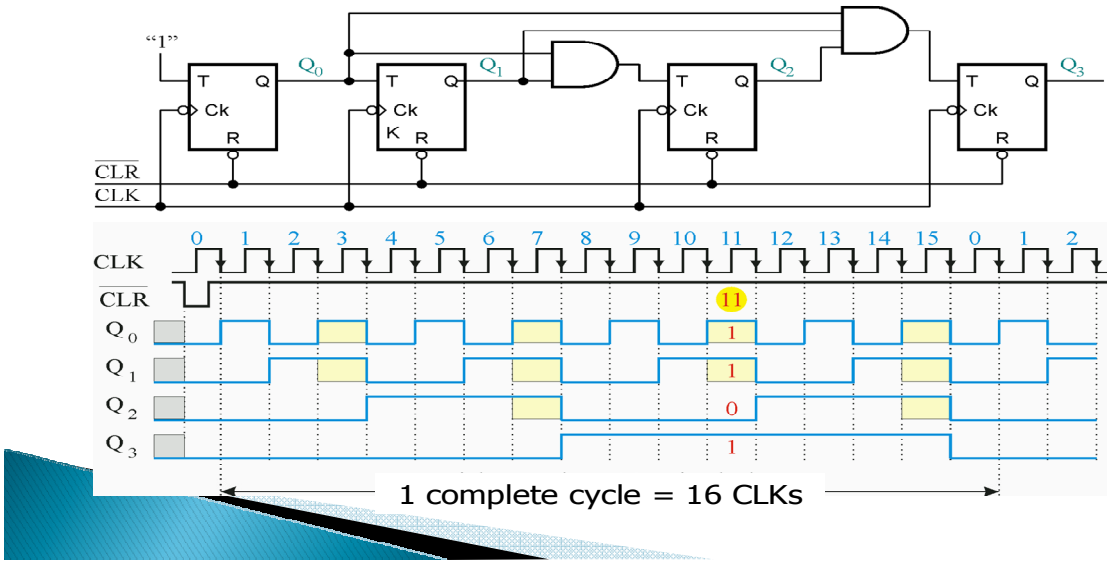
- Counters slide 34 - 39



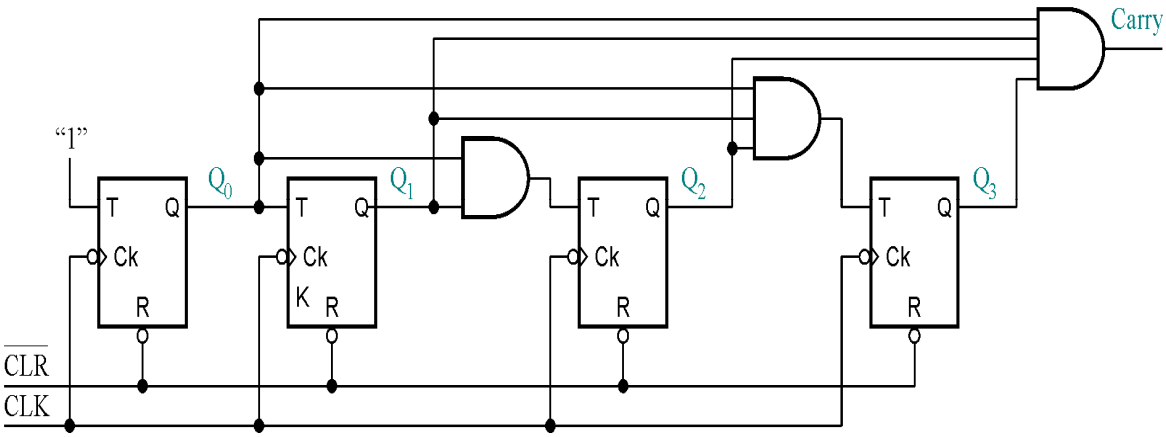
- The counter structure previous presented is sometimes called a *synchronous serial counter* because the combinational enable signals propagate serially from the least significant to the most significant bits.
- If the clock period is too short, there may not be enough time for a change in the counter's LSB to propagate to the MSB.
- This problem is eliminated by driving each EN input with a dedicated AND gate, just a single level of logic.
- Called a *synchronous parallel counter,* this is the *fastest binary counter* structure.



Synchronous Parallel Counter



- Adding Output Carry Feature

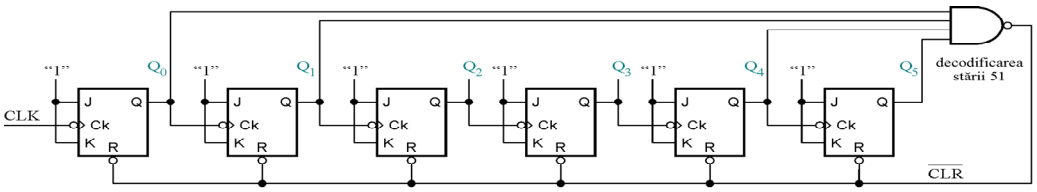


7. Outline the main methods for obtaining modulus p frequency dividers and programmable frequency dividers

- Counters slide 24 - 29

Modulus *p* Counter Design

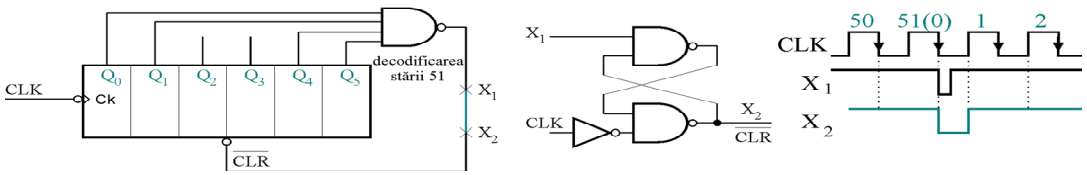
- Let p = 51
- There are $\log_2 51 = 6$ flip flops needed
- $p = 51 = 1*32 + 1*16 + 0*8 + 0*4 + 1*2 + 1*1$
- $p = 110011_2$



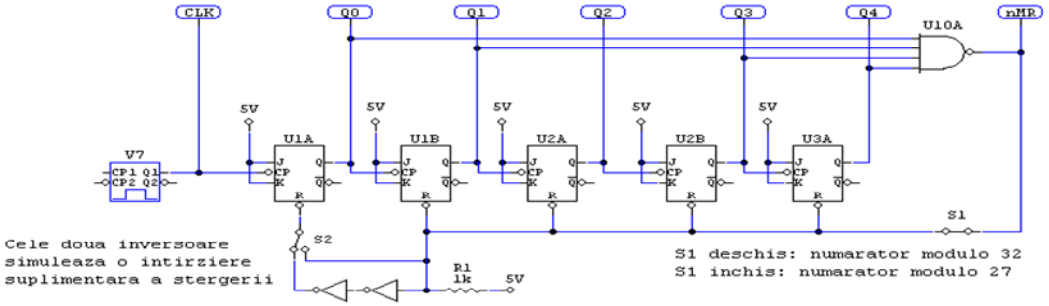
32	16	8	4	2	1
$Q_5 = 1$	$Q_4 = 1$	$Q_3 = 0$	$Q_2 = 0$	$Q_1 = 1$	$Q_0 = 1$

Modulus *p* Counter Design

- A latch to store the internal nCLR signal is needed

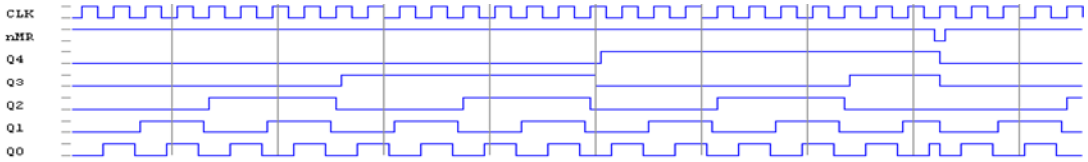


Simulation for p = 27

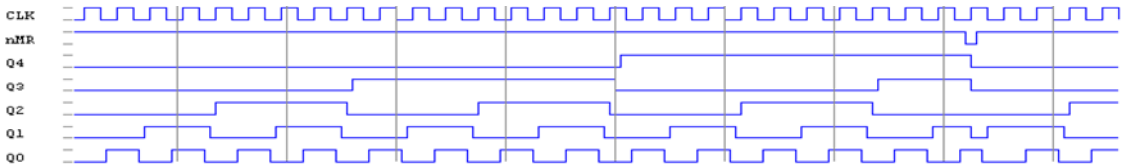


Ripple counter (p = 27) – simulated delayed Reset signal

Simulation for p = 27

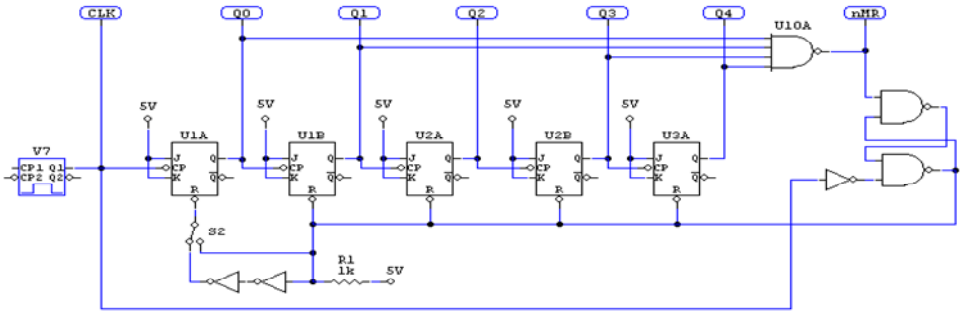


Modulus 27 counter, correct timing (S1 ON, S2 – to right)



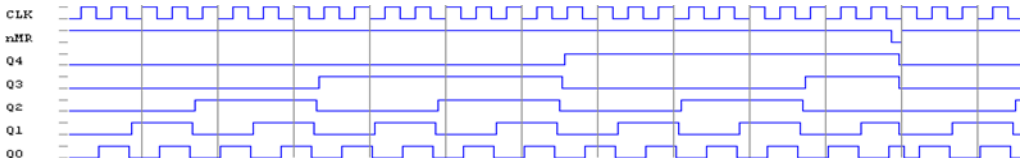
Modulus 27 counter, incorrect timing (S1 ON, S2 – to left)
Sequence is ...26, 27+ CLR, 2, 3, ...

Adding the SR Latch



Schematic

Correct timing

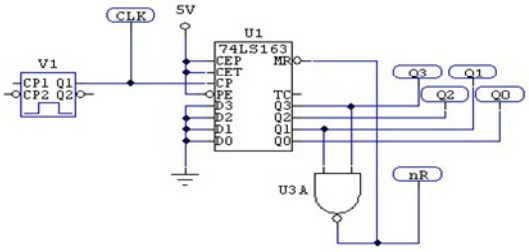


S1 ON, S2 to left

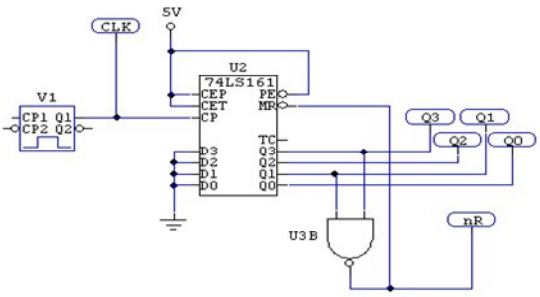
8. Influence of Sync / Async Reset (explain using waveforms and a 74x163 based counter.

- Counters slide 63 - 64.

Influence of Sync / Async Reset

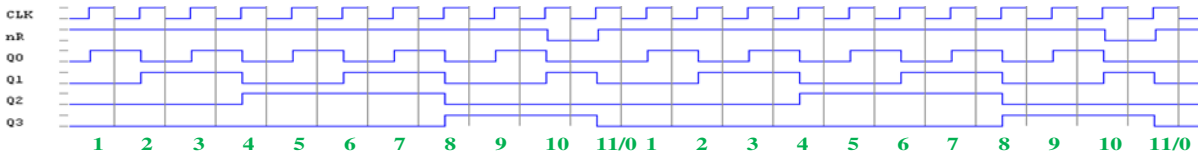


74x163 - Synchronous Reset
Modulus = 11

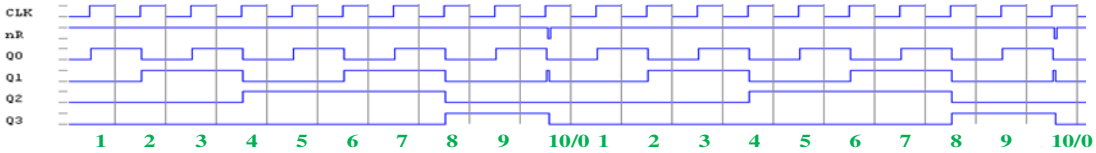


74x161 - Asynchronous Reset
Modulus = 10

Influence of Sync / Async Reset - Waveforms



74x163 - Synchronous Reset – Modulus = 11

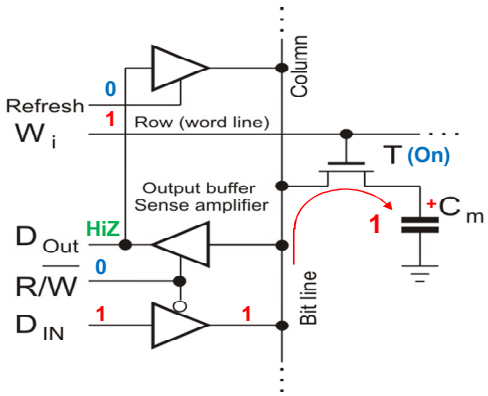


74x161 - Asynchronous Reset – Modulus = 10

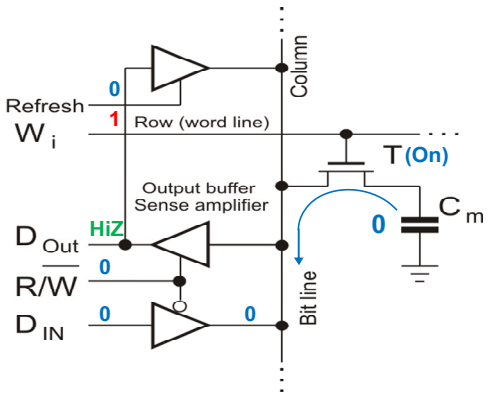
9. Explain briefly the operation of a DRAM - reading, writing, refresh

- Memories slide 96-98

DRAM – Write Operation

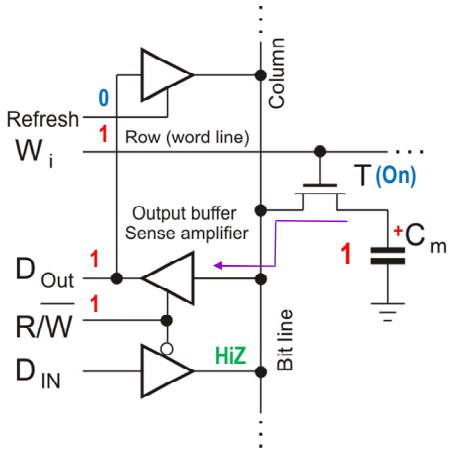


*Writing a **1** into the memory cell*

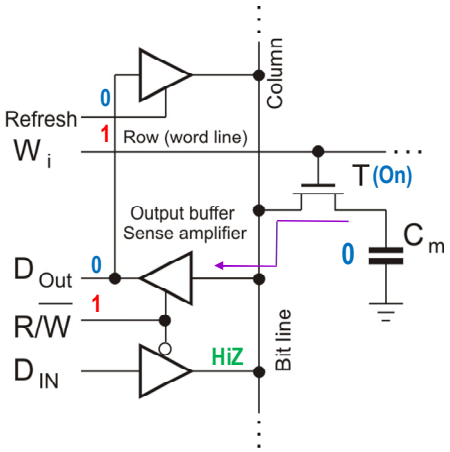


*Writing a **0** into the memory cell*

DRAM – Read Operation

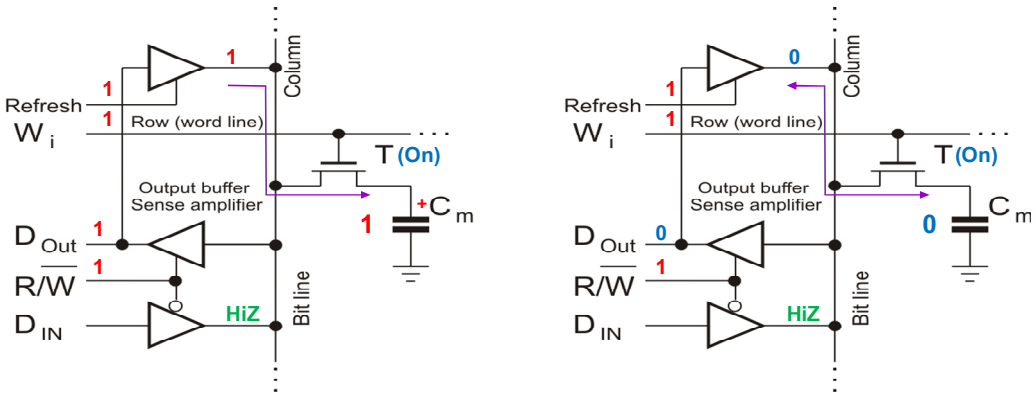


*Reading a **1** from the memory cell*



*Reading a **0** from the memory cell*

DRAM – Refresh Operation



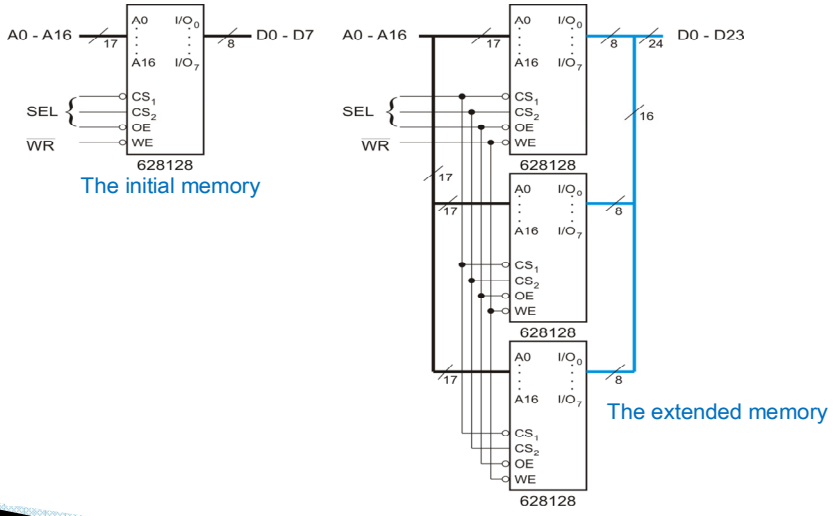
*Refreshing a stored **1***

*Refreshing a stored **0***

10. Memory extension techniques

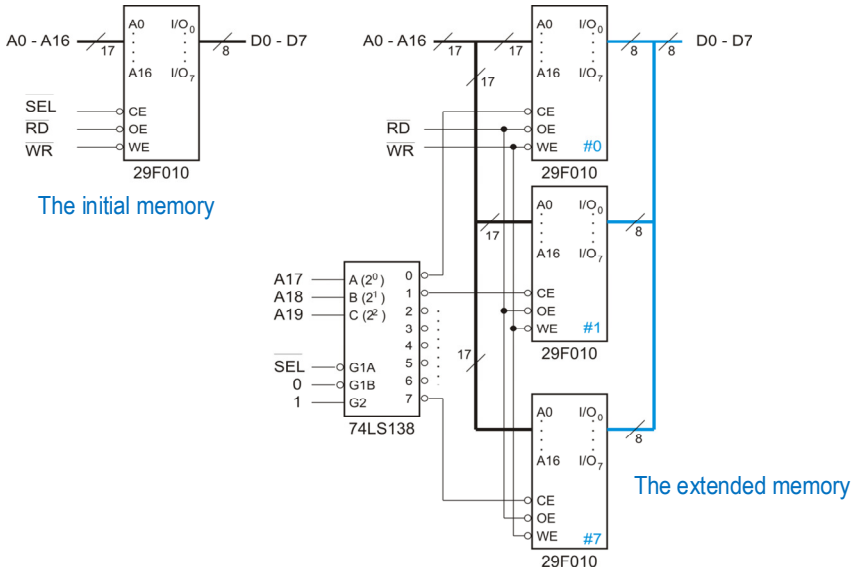
- Memories slide 106 - 109

Extending the Word Width



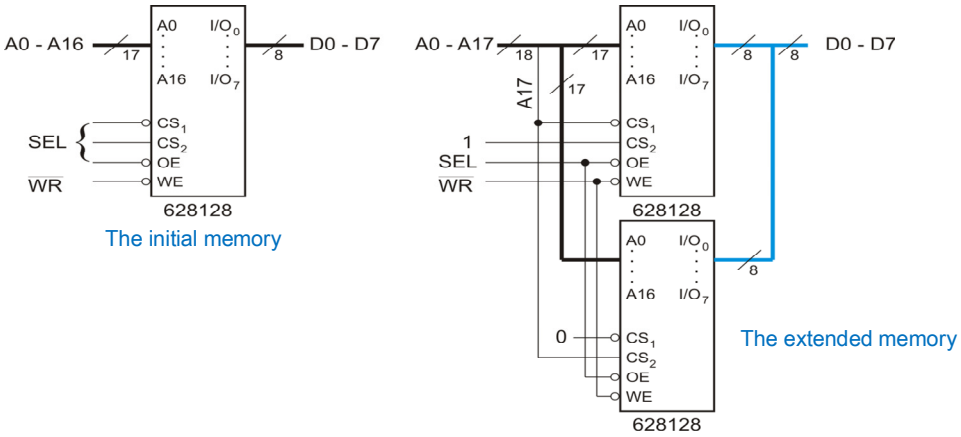
Word width extension 8 -> 24 bits

Extending the Number of Words



Extending the number of words (128 x 8 -> 1024 x 8 kbit)

Extending the Number of Words



Doubling the capacity (128 to 256 kB)

Mixed Extension

Mixed extension: 128 k x 8 bit -> 256 k x 12 bit