Analog Integrated Circuits

1. **CC-CE, CC-CC and Darlington configurations - name the main parameters most often used to characterize these circuits. pg. 204 course #2**

The common-collector - common-emitter (CC-CE), common-collector-common-collector (CC-CC), and ~arlingtonco~n figurations are all closely related. They incorporate an additional transistor to boost the current gain and input resistance of the basic bipolar transistor. The common-collector-common-emitter configuration is shown in Fig. 1. The biasing current source I_{BIAS} is present to establish the quiescent dc operating current in the emitter-follower transistor Q1; th is current source may be absent in some cases or may be replaced by a resistor.

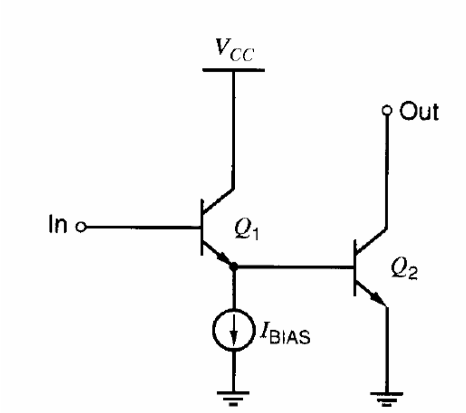


Fig. 1 CC-CE

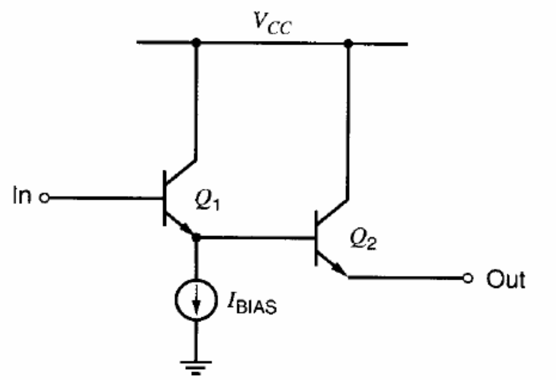


Fig. 2 CC-CC

The common-collector-common-collector configuration is illustrated in Fig. 2. In both of these configurations, the effect of transistor Ql is to increase the current gain through the stage and to increase the input resistance.

The Darlington configuration, illustrated in Fig. 3, is a composite two-transistor device in which the collectors are tied together and the emitter of the first device drives the base of the second. A biasing element of some sort is used to control the emitter current of Ql. The result is a three-terminal composite transistor that can be used in place of a single transistor in common-emitter, common-base, and common-collector configurations. When used as an emitter follower, the device is identical to the CC-CC connection already described. When used as a common-emitter amplifier, the device is very similar to the CC-CE connection, except that the collector of Ql is connected to the output instead of to the power supply. One effect of this change is to reduce the effective output resistance. Also, this change increases the input capacitance because of the connection of the collector-base capacitance of Ql from the input to the output. Because of these drawbacks, the CC-CE connection is normally preferable in integrated small-signal amplifiers. The term *Darlington* is often used to refer to both the CC-CE and CC-CC connections.

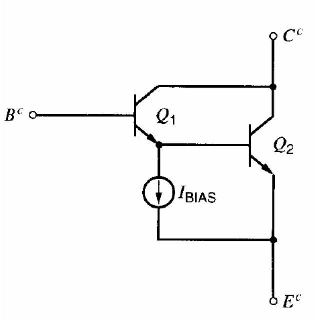


Fig. 3 Darlington configuration

2. **The bipolar cascode configuration – draw the circuit, compare its output resistance with that of the common emitter stage. pg. 207, course #2**

In bipolar form, the cascode is a common-emitter-common-base (CE-CB) amplifier, as shown in Fig. 4.

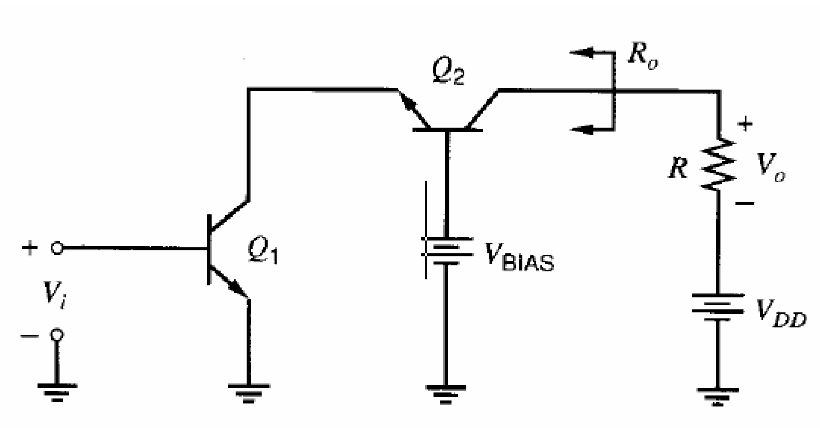


Fig. 4 Bipolar cascode amplifier

Therefore, the CE-CB connection displays an output resistance that is larger by a factor of about β_0 than the CE stage alone.

3. **The dc transfer characteristic of an emitter-coupled pair - compare the schemes with and without emitter degeneration. pg. 215 – 217 (abstract), course #2.**

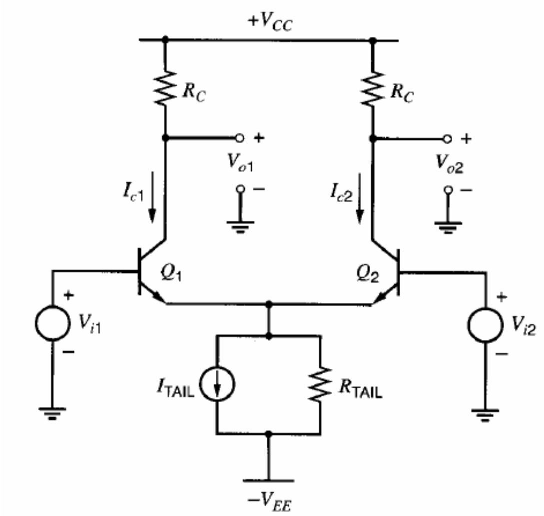


Fig. 5 Emitter-coupled pair circuit diagram.

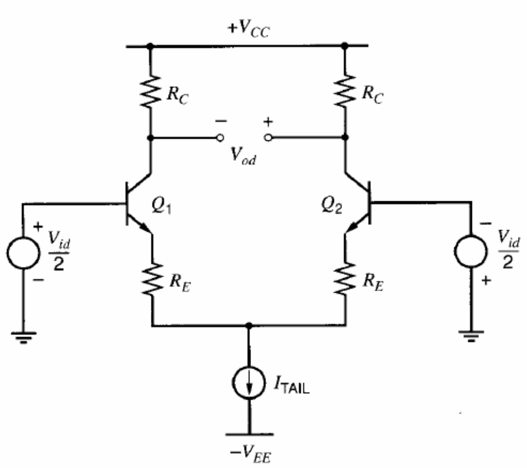


Fig. 6 Emitter-coupled pair with emitter degeneration.

To increase the range of Vid over which the emitter-coupled pair behaves approximately as a linear amplifier, emitter-degeneration resistors are frequently included in series with the emitters of the transistors, as shown in Fig. 6. For large values of emitter-degeneration resistors, the linear range of operation is extended by an amount approximately equal to $I_{TAIL}R_E$. This result stems from the observation that all of I_{TAIL} flows in one of the degeneration resistors when one transistor turns off. Therefore, the voltage drop is $I_{TAIL}R_E$ on one resistor and zero on the other, and the value of Vid required to turn one transistor off is changed by the difference of the voltage drops on these resistors. The voltage gain is reduced by approximately the same factor that the input range is increased. In operation, the emitter resistors introduce local negative feedback in the differential pair.

4. **Simple current mirror - bipolar version. Draw the schematic and compare it with an ideal current mirror. pg. 256, course #4**

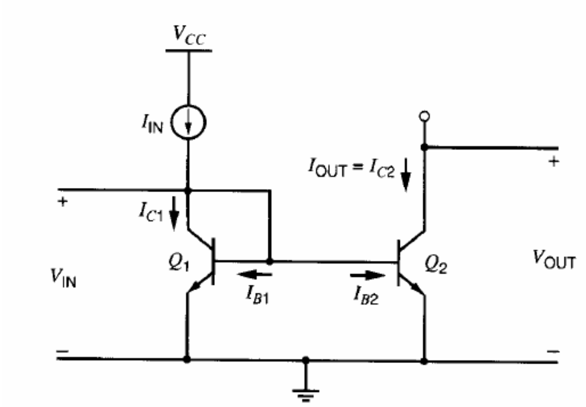


Fig. 7 A simple bipolar current mirror.

A current mirror is an element with at least three terminals, as shown in Fig. 7. The common terminal is connected to a power supply, and the input current source is connected to the input terminal. Ideally, the output current is equal to the input current multiplied by a desired current gain. If the gain is unity, the input current is reflected to the output, leading to the name ***current mirror.*** Under ideal conditions, the current-mirror gain is independent of input frequency, and the output current is independent of the voltage between the output and common terminals. Furthermore, the voltage between the input and common terminals is ideally zero because this condition allows the entire supply voltage to appear across the input current source, simplifying its transistor-level design. In practice, real transistor-level current mirrors suffer many deviations from this ideal behavior. For example, the gain of a real current mirror is never independent of the input frequency. One of the most important deviations from ideality is the variation of the current mirror output current with changes in voltage at the output terminal. This effect is characterized by the small-signal output resistance, R,, of the current mirror. Another important error source is the gain error, which is the deviation of the gain of a current mirror from its ideal value.

5. **Wilson current mirror – draw the schematic, estimate the value of the output resistance and compare it with that of the cascode current mirror. pg. 277, Course #6**

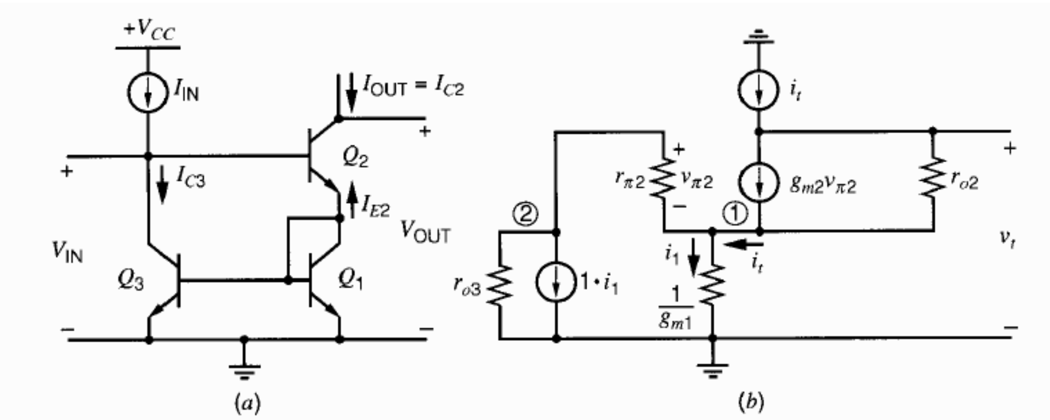


Fig. 8 a) Bipolar Wilson current mirror. b Small signal model

This circuit uses negative feedback through Ql, activating Q3 to reduce the base-current error and raise the output resistance.

If $r_{o3} \to \infty$ the small-signal current that flows in the collector of Q_3 is equal to i_1 and the output resistance is

$$R_o = \frac{1}{g_{m1}(2)} + r_{o2} + \frac{g_{m2} r_{\pi 2} r_{o2}}{2} \simeq \frac{\beta_0 r_{o2}}{2}$$

This result is the same as for the cascode current mirror.

6. **Bipolar Widlar Current Source - draw the schematic, explain why it is not a current mirror. pg. 300, course #8**

In ideal operational amplifiers, the current is zero in each of the two input leads. However, the input current is not zero in real op amps with bipolar input transistors because β_F is finite. Since the op-amp inputs are usually connected to a differential pair, the tail current must usually be very small in such op amps to keep the input current small. Typically, the tail current is on the order of *5* μA**.** Currents of such low magnitude can be obtained with moderate values of resistance, however, by modifying the simple current mirror so that the transistors operate with unequal base-emitter voltages. In the Widlar current source of Fig. 9, resistor R_2 is inserted in series with the emitter of Q2, and transistors Q1 and Q2 operate with unequal base emitter voltages if $R_2 \neq 0$. This circuit is referred to as a current source rather than a current mirror because the output current is much less dependent on the input current and the power-supply voltage than in the simple current mirror.

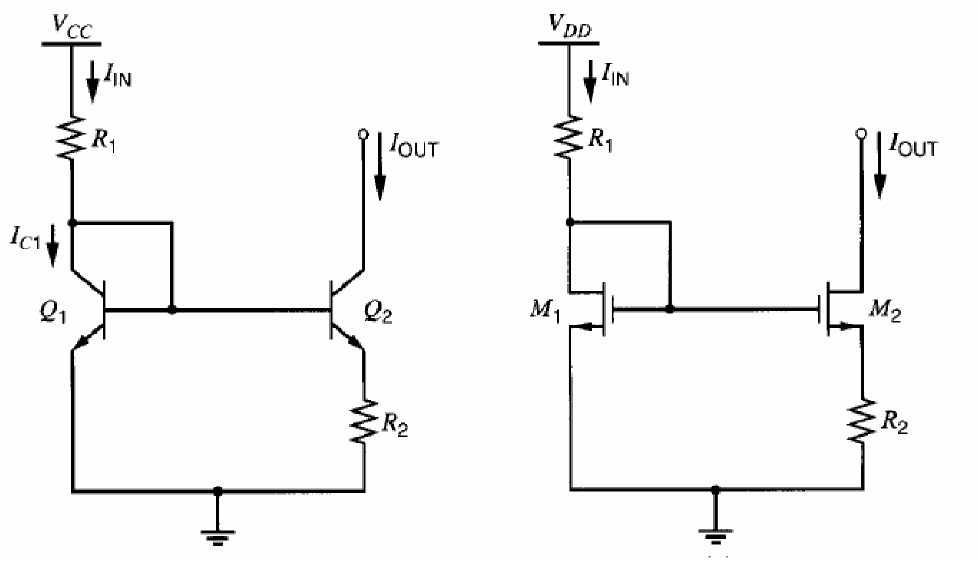


Fig. 9 Widlar current sources: bipolar and MOS.

7. **Temperature-Insensitive Bias with band gap voltage reference: the idea, one of the practical implementations. pg. 317, course #9**

Since the bias sources referenced to V_{BE}(on) and V_T have opposite TC_F, the possibility exists for referencing the output current to a composite voltage that is a weighted sum of V_{BE}(on) and V_T. By proper weighting, zero temperature coefficient should be attainable. In the biasing sources described so far, we have concentrated on the problem of obtaining a *current* with low temperature coefficient. In practice, requirements often arise for low-temperature-coefficient voltage bias or reference *voltages*. The voltage reference for a voltage regulator is a good example.

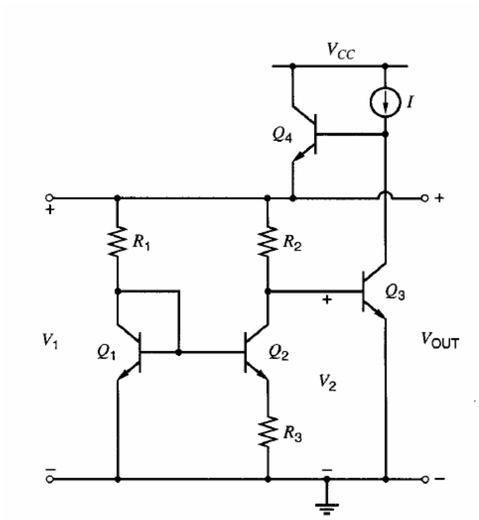


Fig. 10 Widlar band-gap reference.

A practical realization of band-gap reference, in bipolar technologies, takes the form illustrated in Fig. 10. This circuit uses a feedback loop to establish an operating point in the circuit such that the output voltage is equal to a VB plus a voltage proportional to the difference between two base-emitter voltages.

8. **Inverting and noninverting amplifier built with an op amp - draw the schematics and find the gains, define the characteristics of an ideal op amp. pg. 406, 408, course #9**

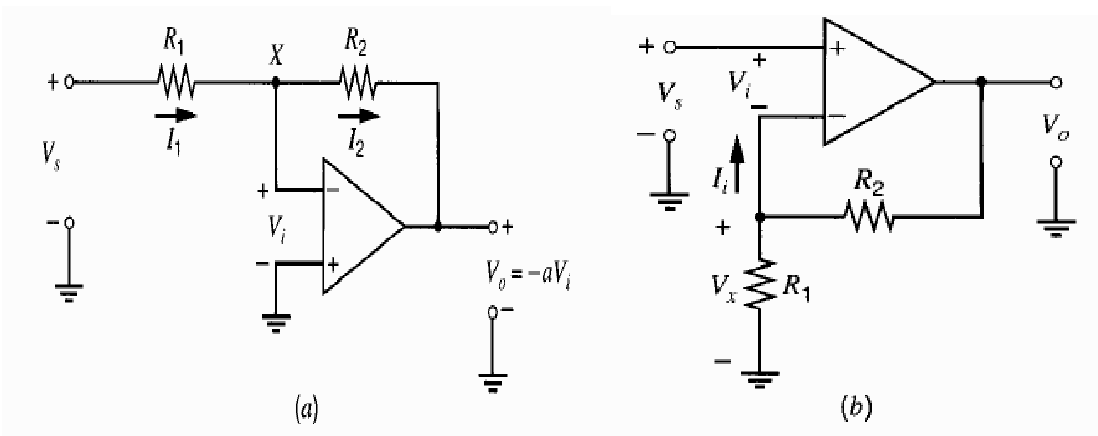


Fig. 11 a) Inverting amplifier; b) Non-inverting amplifier

The inverting amplifier connection is shown in Fig. 11 a. We assume that the op-amp input resistance is infinite, and that the output resistance is zero. From KCL at node X:

$$\frac{V_s - V_i}{R_1} + \frac{V_o - V_i}{R_2} = 0$$

Since R_2 is connected between the amplifier output and the inverting input, the feedback is negative. Therefore, V_i would be driven to zero with infinite open-loop gain. On the other hand, with finite open-loop gain *a*,

$$V_i = \frac{-V_o}{a}$$

It results that: $$\frac{V_o}{V_s} = -\frac{R_2}{R_1}\left[\frac{1}{1 + \frac{1}{a}\left(1 + \frac{R_2}{R_1}\right)}\right]$$

If the gain of the op amp is large enough that $$a\left(\frac{R_1}{R_1 + R_2}\right) \gg 1$$

then the closed-loop gain is $$\frac{V_o}{V_s} \simeq -\frac{R_2}{R_1}$$

The noninverting amplifier is shown in Fig 11b. We assume that no current flows into the inverting op-amp input terminal. If the open-loop gain is a, $V_i = V_0/a$ and

$$V_x = V_o\left(\frac{R_1}{R_1 + R_2}\right) = V_s - \frac{V_o}{a}$$

Rearranging gives:

$$\frac{V_o}{V_s} = \left(1 + \frac{R_2}{R_1}\right)\frac{\dfrac{aR_1}{R_1 + R_2}}{1 + \dfrac{aR_1}{R_1 + R_2}} \simeq \left(1 + \frac{R_2}{R_1}\right)$$

In contrast to the inverting case, this circuit displays a very high input resistance as seen by V_s. Also unlike the inverting case, the noninverting connection causes the common-mode input voltage of the op amp to be equal to V_s.

9. **Integrator, differentiator build with op amp - draw the schematics, find the relationships between input and output voltages. pg. 410, Course #10**

The integrator and differentiator circuits, shown in Fig. 12, are examples of using op amps with reactive elements in the feedback network to realize a desired frequency response or time-domain response.

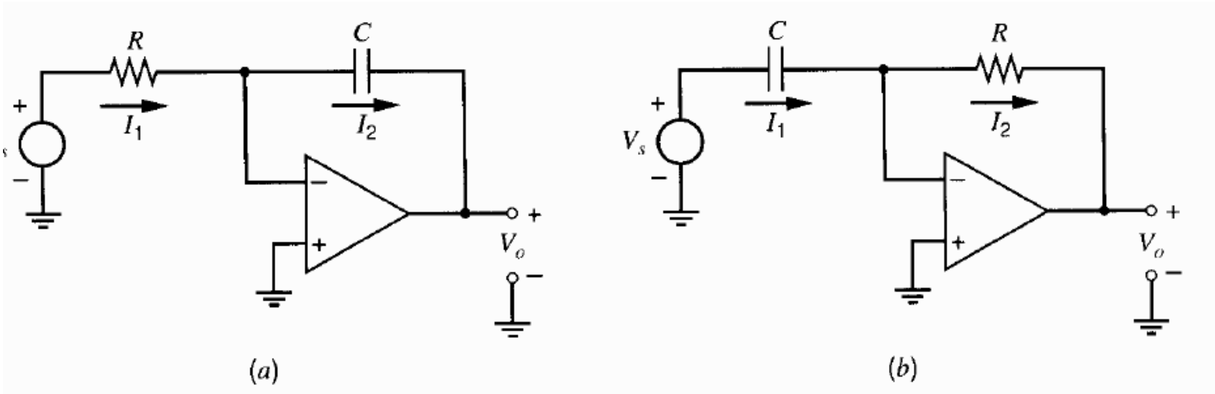


Fig. 12 a) Integrator configuration b) Differentiator configuration

In the case of the integrator, the resistor *R* is used to develop a current I_1 that is proportional to the input voltage. This current flows into the capacitor C, whose voltage is proportional to the integral of the current *Il* with respect to time. Since the output voltage is equal to the negative of the capacitor voltage, the output is proportional to the integral of the input voltage with respect to time. In terms of equations:

$$I_1 = \frac{V_s}{R} = I_2$$

and

$$V_o = -\frac{1}{C}\int_0^t I_2 d\tau + V_o(0)$$

It results that:

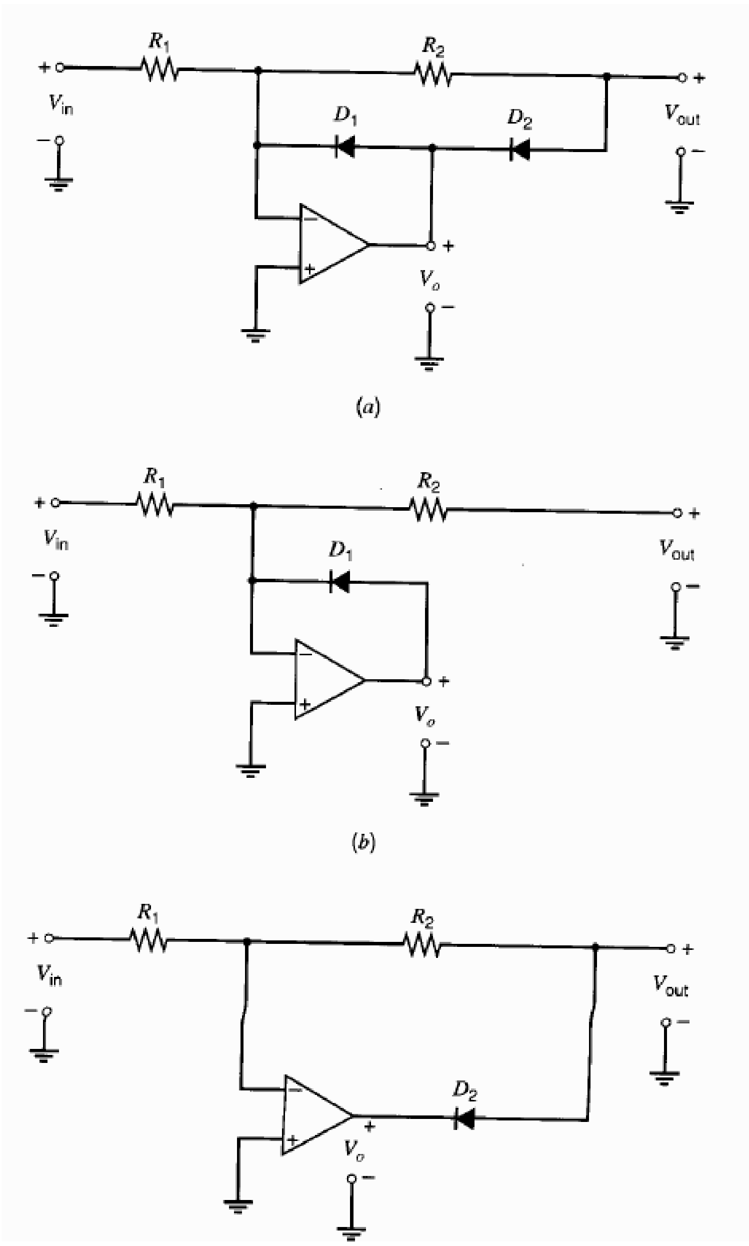
$$V_o(t) = -\frac{1}{RC}\int_0^t V_s(\tau)d\tau + V_o(0)$$

In the case of the differentiator, the capacitor C is connected between V_s, and the inverting op-amp input. The current through the capacitor is proportional to the time derivative of the voltage across it, which is equal to the input voltage. This current flows through the feedback resistor R, producing a voltage at the output proportional to the capacitor current, which is proportional to the time rate of change of the input voltage. In terms of equations:

$$I_1 = C\frac{dV_s}{dt} = I_2$$

$$V_o = -RI_2 = -RC\frac{dV_s}{dt}$$

10. **Improved precision half-wave rectifier - draw the schematics, explain the operation. pg.705, Course #10.**



(c)

Fig. 13 Improved precision rectifier. a) Rectifier circuit b) Equivalent circuit for $V_{in}<0$ c) Equivalent circuit for $V_{in}>0$

Diode D_1 is forward biased and the op amp is in the active region. The inverting input of the op amp is clamped at ground by the feedback through D_1, and, since no current flows in R_2, the output voltage is also at ground. When the input voltage is made positive, no current can flow in the reverse direction through D_1 so the output voltage of the op amp V_o, is driven in the negative direction. This reverse biases D_1 and forward biases D_2. The resulting equivalent circuit is shown in Fig. 13 c and is simply an inverting amplifier with a forward-biased diode in series with the output lead of the op amp. Because of large gain of the op amp, this diode has no effect on its behavior as long as it is forward biased, and so the circuit behaves as an inverting amplifier giving an output voltage

$$V_{out} = -\frac{R_2}{R_1} V_{in}$$

Signal Processing

1- Where are the poles of a stable and causal analog system? Give an example.
http://shannon.etc.upt.ro/teaching/sp-pi/Course/1_Laplace.pdf slide 62

The degree of numerator of a transfer function for an impulse response with no unit impulse in origin= **less** than the degree of denominator **with at least one**.

If $M+1>N$, $h(t)$ contains unit impulse in origin

Example

$$H_u(s)=\frac{s+2}{s+1}=1+\frac{1}{s+1} \qquad h(t)=\delta(t)+e^{-t}\sigma(t).$$

number of poles of H(s) is greater than the number of zeros with at least one.

causal stable system :
poles **in the left half plane LHP,**
its zeros anywhere in the complex plane.

62

2- Define minimum phase analog systems. Give an example.
http://shannon.etc.upt.ro/teaching/sp-pi/Course/1_Laplace.pdf slide 63

minimum phase systems: poles and zeros in the left half plane.

Example. $h(t)=e^{-t}\sigma(t)\leftrightarrow H_u(s)=\frac{1}{s+1}.$

-a pole in the left half plane.

- No zeros $\Rightarrow$minimum phase system.

The frequency response

$$H(\omega)=1/(1+j\omega),$$

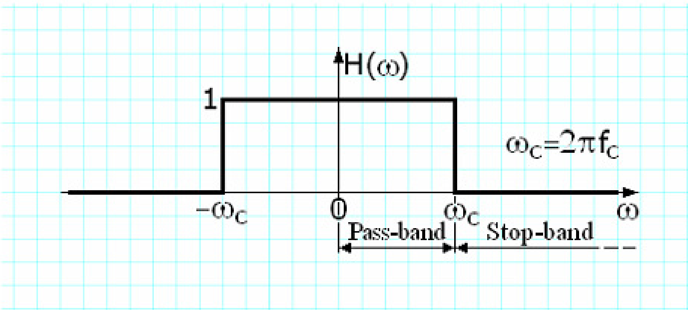
frequency characteristics

$$|H(\omega)|=1/\sqrt{1+\omega^2}, \qquad \Phi(\omega)=-arctg\omega.$$

3- Ideal low pass filter.
http://shannon.etc.upt.ro/teaching/sp-pi/Course/2_Filtering.pdf slide 6

- Ideal low pass filter

$$H(\omega) = p_{\omega_c}(\omega) \leftrightarrow h(t) = \frac{\sin \omega_c t}{\pi t}$$



4- Enunciate WKS sampling theorem.
http://shannon.etc.upt.ro/teaching/sp-pi/Course/3_Sampling.pdf slide 17

If the finite energy signal $x(t)$ is band limited at ω_M, ($X(\omega)=0$ for $|\omega| > \omega_M$), it is uniquely determined by its samples $\{x(nT_s) | n \in \mathbb{Z}\}$ if the sampling frequency is higher or equal than twice the maximum frequency of the signal:

$$\omega_s \geq 2\omega_M$$

the original signal can be reconstructed from its samples a.e.w:

$$x_r(t) = \sum_{k=-\infty}^{\infty} \frac{2\omega_c}{\omega_s} x(kT_s) \frac{\sin \omega_c (t - kT_s)}{\omega_c (t - kT_s)}$$

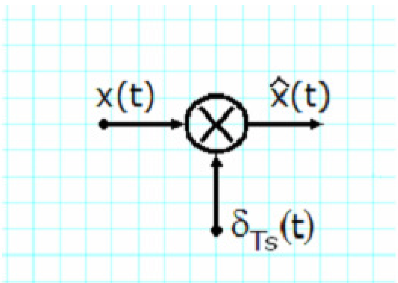
if the cut-off frequency of ideal low-pass reconstruction filter :

$$\omega_M \leq \omega_c \leq \omega_s - \omega_M$$

17

5- Spectrum of ideal sampled signal (Relation + Graphical representation).

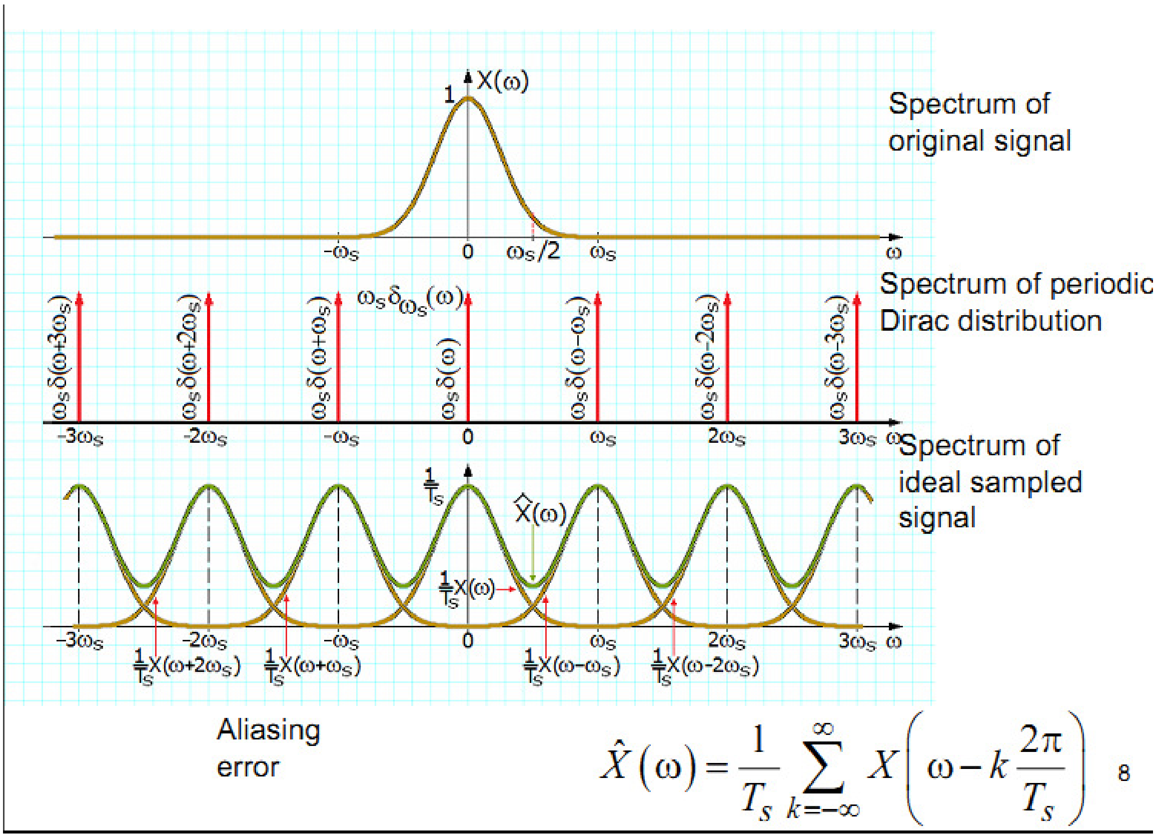
http://shannon.etc.upt.ro/teaching/sp-pi/Course/3_Sampling.pdf slide 7,8



$$\hat{x}(t) = \sum_{k=-\infty}^{\infty} x(kT_s)\delta(t - kT_s)$$

$$\hat{X}(\omega) = \frac{1}{T_s}\sum_{k=-\infty}^{\infty} X\left(\omega - k\frac{2\pi}{T_s}\right)$$

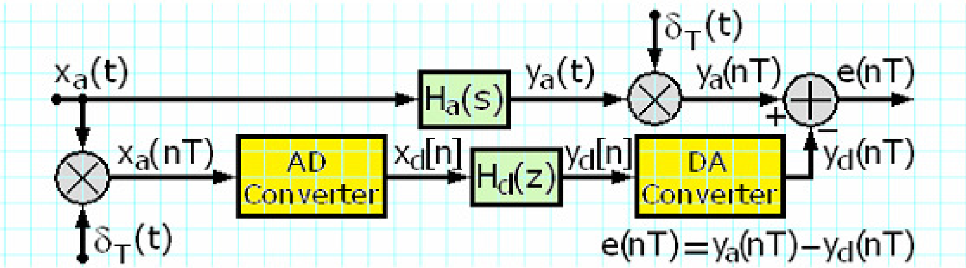
The spectrum of an ideal sampled signal is the periodic repetition of the spectrum of the original signal. The period is inverse proportional with the sampling step T_s.



6- Approximation of continuous-time systems with discrete-time systems using impulse invariance method.

http://shannon.etc.upt.ro/teaching/sp-pi/Course/5_Approximation.pdf slide 7

$$\boxed{h_d[n] = Th_a(nT)}$$



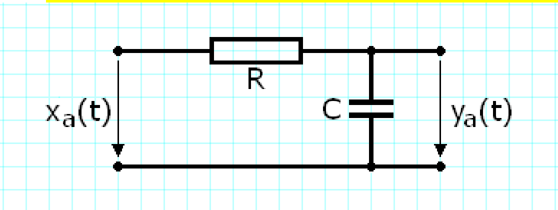
$$y_a(t) = h_a(t) \;;\; x_d[n] = \frac{1}{T}\delta[n].$$

$$y_a(nT) = h_a(nT)$$

$$y_d[n] = \frac{1}{T}\delta[n] * h_d[n] = \frac{1}{T}h_d[n]$$

$$\text{Minimum error } e(nT) \;: h_a(nT) = \frac{1}{T}h_d(nT)$$ 7

7- Approximation of RC circuit using bilinear transform method.



http://shannon.etc.upt.ro/teaching/sp-pi/Course/5_Approximation.pdf slide 38, 43

$$\text{time constant:}\tau = RC = \frac{1}{\omega_0}.$$

$$H_a(s) = \frac{1}{1+s\tau}$$

$$H_d(z) = \frac{\dfrac{T}{T+\tau}}{1-\dfrac{\tau}{T+\tau}z^{-1}}$$

$$I_n = y(nT) - y((n-1)T) = \int_{(n-1)T}^{nT} x(\tau)d\tau$$

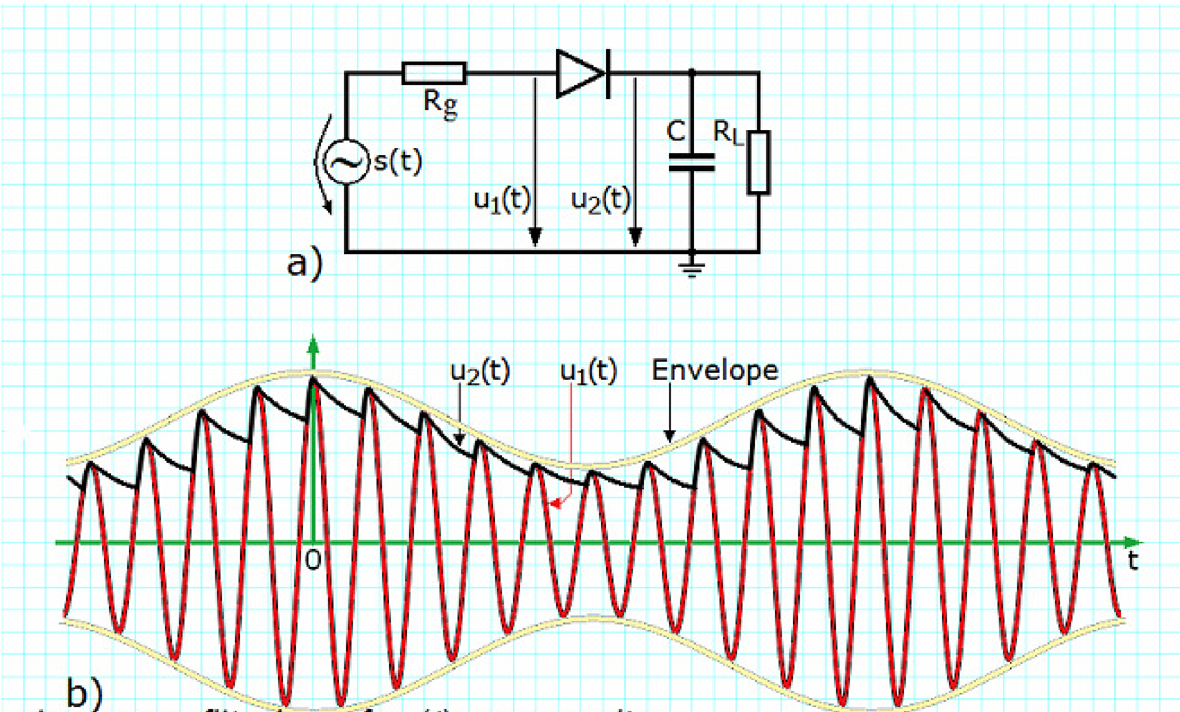
$$\cong \frac{(AB+CD)AD}{2} = \frac{\left[x(nT)+x((n-1)T)\right]T}{2}$$

$$\Rightarrow y[n]-y[n-1] = \frac{T}{2}\left(x[n]+x[n-1]\right)$$

$$H_d(z) = \frac{T}{2}\frac{1+z^{-1}}{1-z^{-1}} = H_a(s)\Big|_{s=\frac{2}{T}\frac{1-z^{-1}}{1+z^{-1}}}$$

8- Demodulator (envelope detector) for AM signals.

http://shannon.etc.upt.ro/teaching/sp-pi/Course/6_Modulation.pdf slide 16



•low-pass filtering of $u_2(t)$ -> capacitor

•removal of the DC component

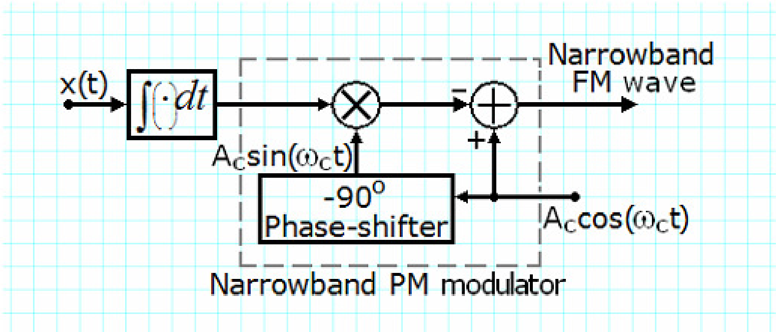
9- Narrow Band Frequency Modulation.

http://shannon.etc.upt.ro/teaching/sp-pi/Course/6_Modulation.pdf slide 49

$$s(t) = A_c \cos\omega_c t \cos(\beta \sin\omega_m t) - A_c \sin\omega_c t \sin(\beta \sin\omega_m t).$$

$$\text{If } \beta < \frac{\pi}{36} \text{ rad } \Rightarrow \cos(\beta \sin\omega_m t) \cong 1 \text{ and } \sin(\beta \sin\omega_m t) \cong \beta \sin\omega_m t$$

$$\Rightarrow s(t) = A_c \cos\omega_c t - \beta A_c \sin\omega_c t \sin\omega_m t.$$



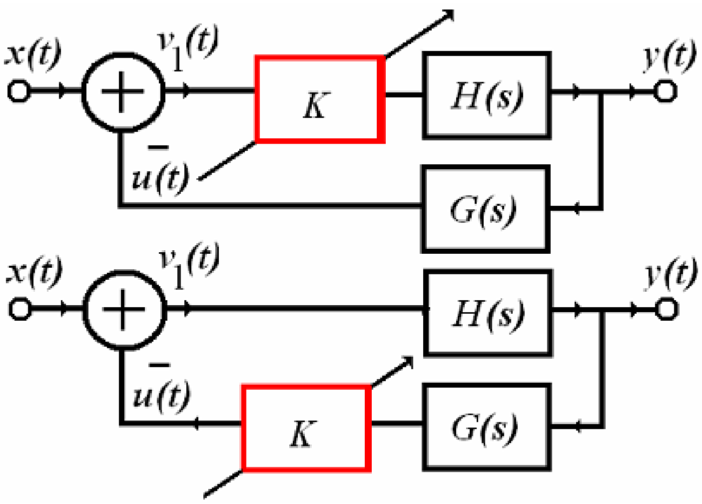
10- Nyquist stability criterion for continuous-time systems when the open loop system is stable (schema + enunciation).

http://shannon.etc.upt.ro/teaching/sp-pi/Course/7_Stability.pdf slide 22(schema), 37 (enunciation)

•Hurwitz: <u>knowledge of closed loop transfer function</u>.

•only H and G can be identified sometimes: i.e. experimental identification of a feedback system

Feedback systems with variable gain



$$\frac{Y(s)}{X(s)} = \frac{KH(s)}{1+KH(s)G(s)}$$

$$\frac{Y(s)}{X(s)} = \frac{H(s)}{1+KH(s)G(s)}$$

1. **If the open loop system is stable** then $H(s)G(s)$ doesn't have poles in the right half plane or on the imaginary axis.

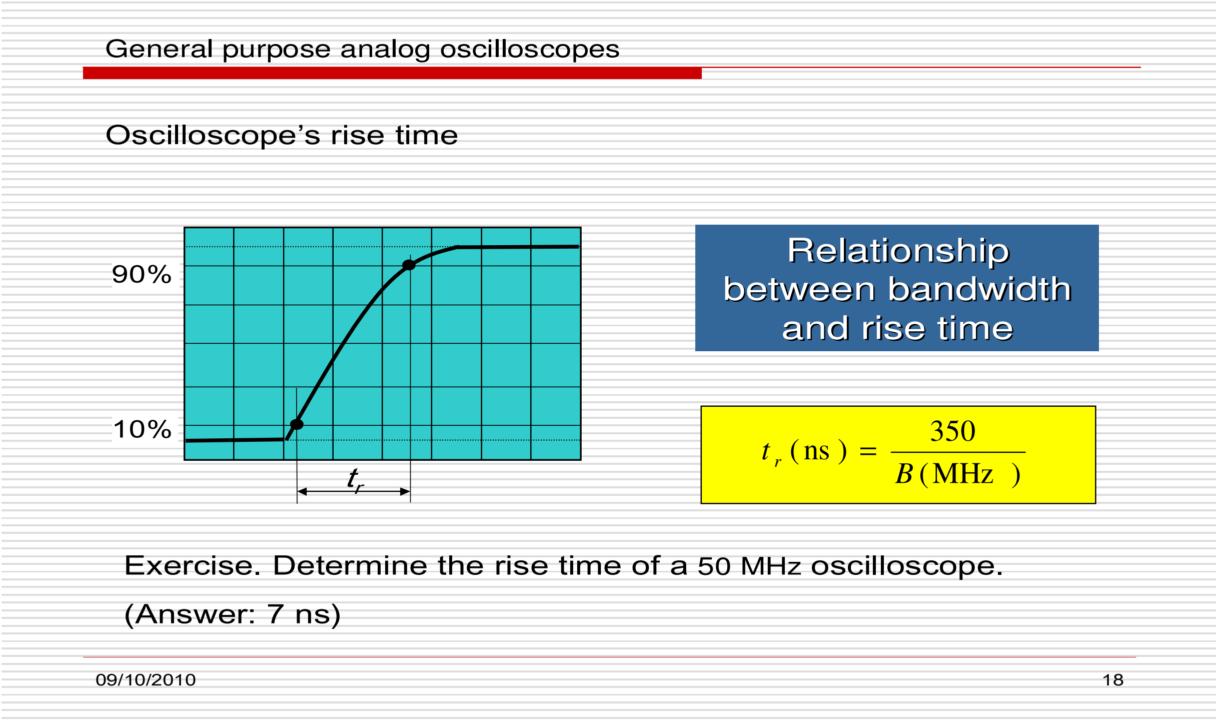
   So, the open loop Nyquist's hodograph **doesn't make complete rotations** around the point (-1/K,0)

2. Since $h(t)$ and $g(t)$ are real functions, Nyquist's hodograph for $\omega \in (-\infty,0)$ is obtained by **symmetry** with respect to the real axis of the complex plane $H(s)G(s)$ from the Nyquist's hodograph for $\omega \in (0,\infty)$

Electronic Instrumentation

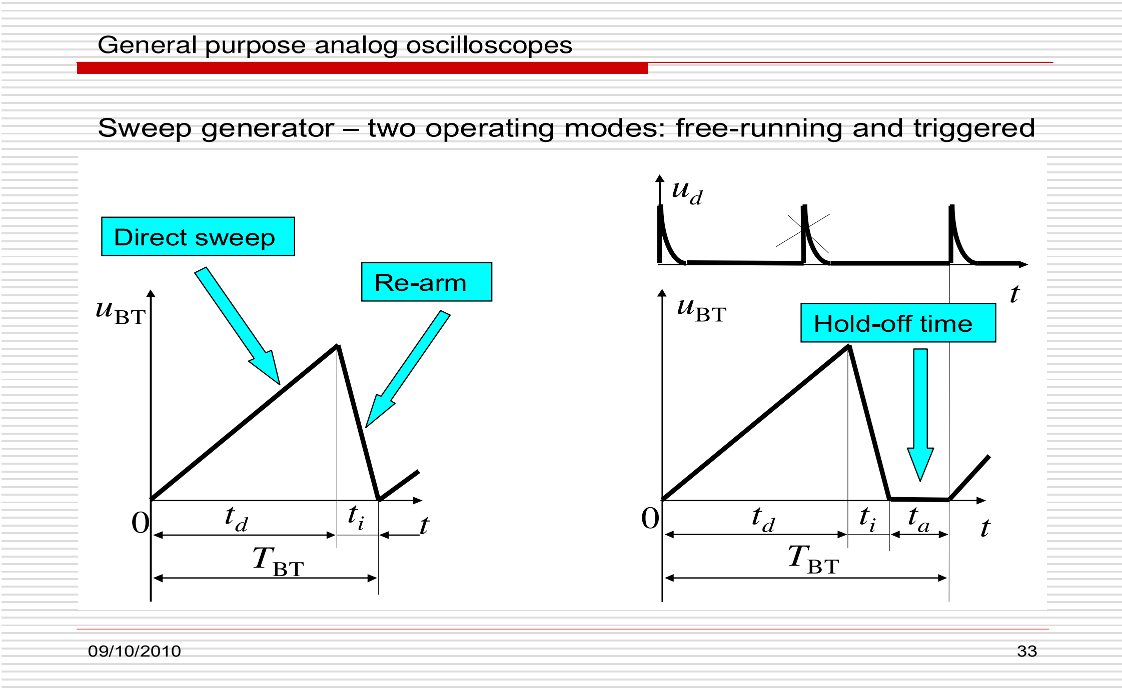
1. **General purpose analog oscilloscopes.** Relationship between bandwidth and rise time of an oscilloscope.

https://intranet.etc.upt.ro/~E_INSTR/PowerPoint%20presentations%202010%202011/1%20Oscilloscopes%202010%202011.ppt , slide #18



2. **General purpose analog oscilloscopes.** Describe the free-running and the triggered modes of operation of the time base.

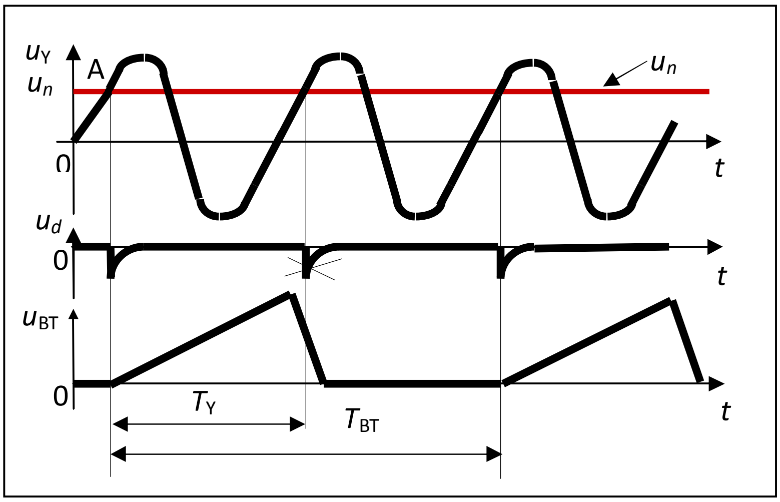
https://intranet.etc.upt.ro/~E_INSTR/PowerPoint%20presentations%202010%202011/1%20Oscilloscopes%202010%202011.ppt, slides #33-38



With triggered sweeps, the scope will blank the beam and start to reset the sweep circuit (re-arm) each time the beam reaches the extreme right side of the screen. For a period of time, called *hold-off*, the sweep circuit resets completely and ignores triggers. Once hold-off expires, the next trigger starts a sweep. The trigger event is usually the input waveform reaching some user-specified threshold voltage (trigger level) in the specified direction (going positive or going negative - trigger polarity). Triggering circuit ensures a stable image on the screen.

Triggering condition $T_{BT} = kT_Y$

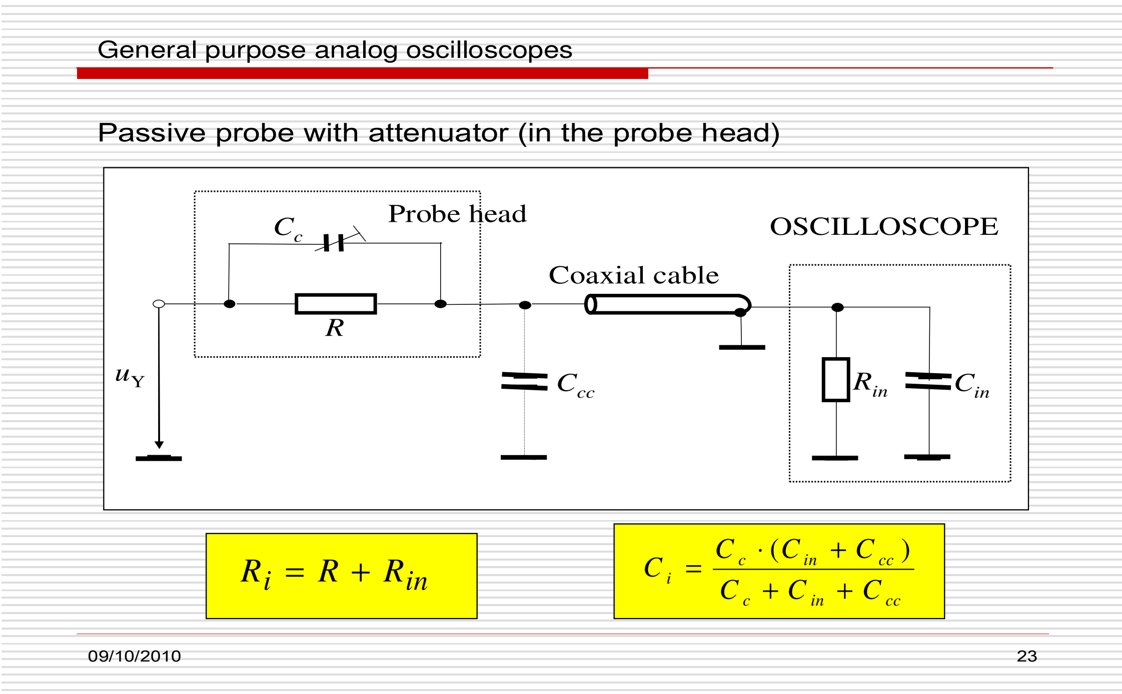
The sweep generator's period should be a multiple of the signal period. Timing diagrams (triggered sweep):



- Oscilloscope mode
  - AUTO
    - sweep generator – free running with no trigger
    - sweep generator – triggered by the trigger signal
  - NORMAL
    - sweep generator – in standby with no trigger
    - sweep generator – triggered by the trigger signal

3. **Probes for oscilloscopes.** Attenuating probes. Frequency compensation. Describe what happens and tell (and draw) how the image of square pulses appears on the screen when the compensation condition is not met.

https://intranet.etc.upt.ro/~E_INSTR/PowerPoint%20presentations%202010%202011/1%20Oscilloscopes%202010%202011.ppt, slides #23-25



Probes without and with attenuator - comparison

Probe without attenuator

- advantage – it does not attenuate the input signal
- disadvantage – relatively small input resistance (1 MΩ), large input capacitance (50 - 150 pF)

Probe with attenuator

- advantage – large input resistance (10 MΩ), small input capacitance (5 - 15 pF)
- disadvantage – it attenuates the input signal (therefore, the value read on the display must be multiplied by the probe's attenuation factor)

4. General purpose analog oscilloscopes. Delayed sweep: use, operating modes, utility.

https://intranet.etc.upt.ro/~E_INSTR/PowerPoint%20presentations%202010%202011/1%20Oscilloscopes%202010%202011.ppt, slides #48-50

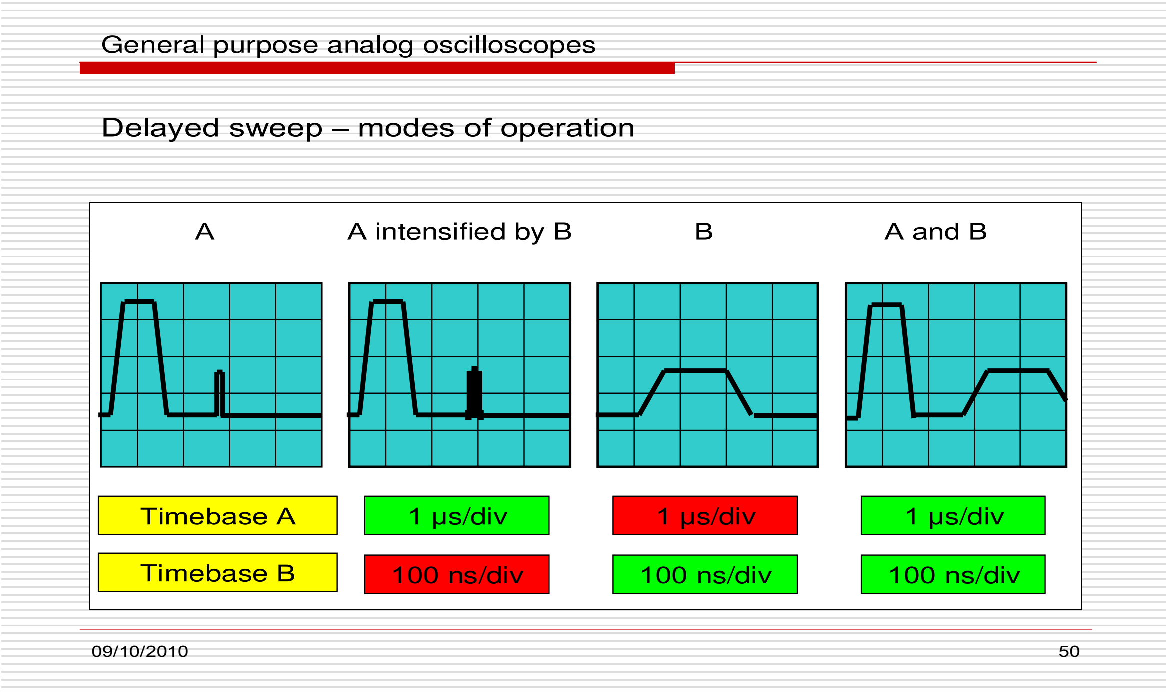
Delayed sweep

- found on more-sophisticated oscilloscopes, which contain a second set of timebase circuits for a delayed sweep.
- provides a very-detailed look at some small selected portion of the main timebase.

The main timebase serves as a controllable delay, after which the delayed timebase starts. This can start when the delay expires, or can be triggered (only) after the delay expires. Ordinarily, the delayed timebase is set for a faster sweep, sometimes much faster, such as 1000:1. At extreme ratios, jitter in the delays on consecutive main sweeps degrades the display, but delayed-sweep triggers can overcome that.

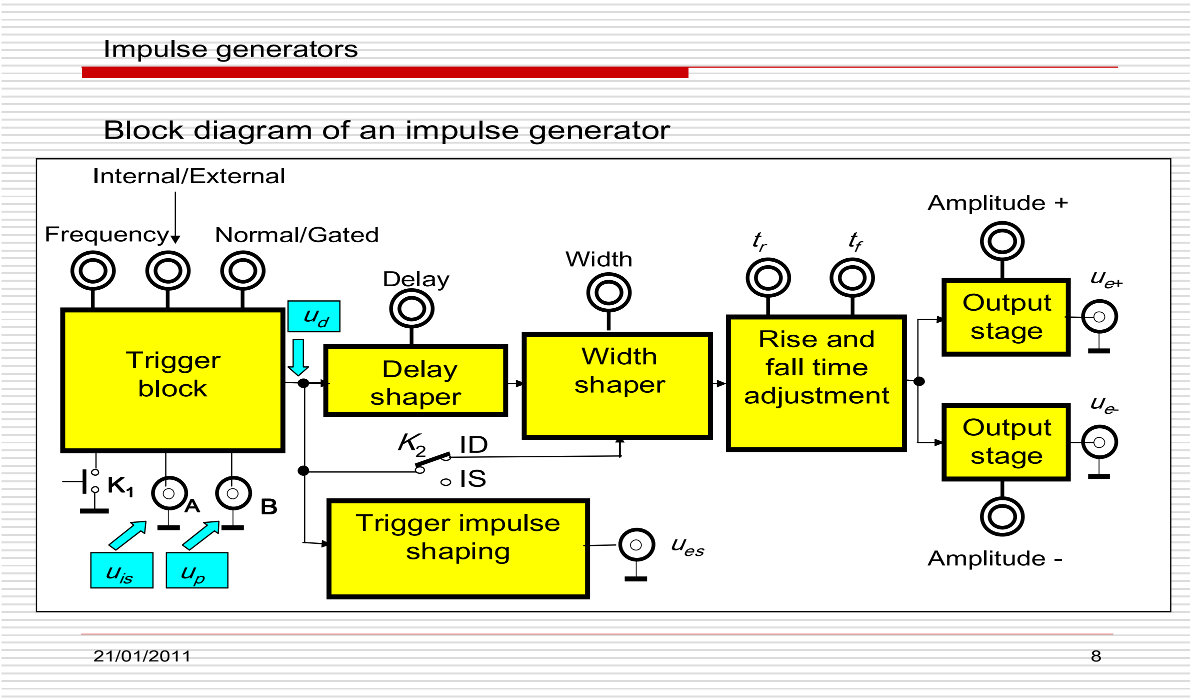
Operating modes

- A
- A intensified by B
- B
- A and B (mixed)



5. Signal generators. Describe the operation of the pulse generator in single and double pulses modes.

https://intranet.etc.upt.ro/~E_INSTR/PowerPoint%20presentations%202010%202011/2%20Signal%20Generators%202010%202011.ppt, slides #8-11



Operating modes

1. NORMAL

- ❑ internally triggered (simple or double impulses)
- ❑ externally triggered (simple or double impulses)
- ❑ single impulses (simple or double impulses)

2. GATED

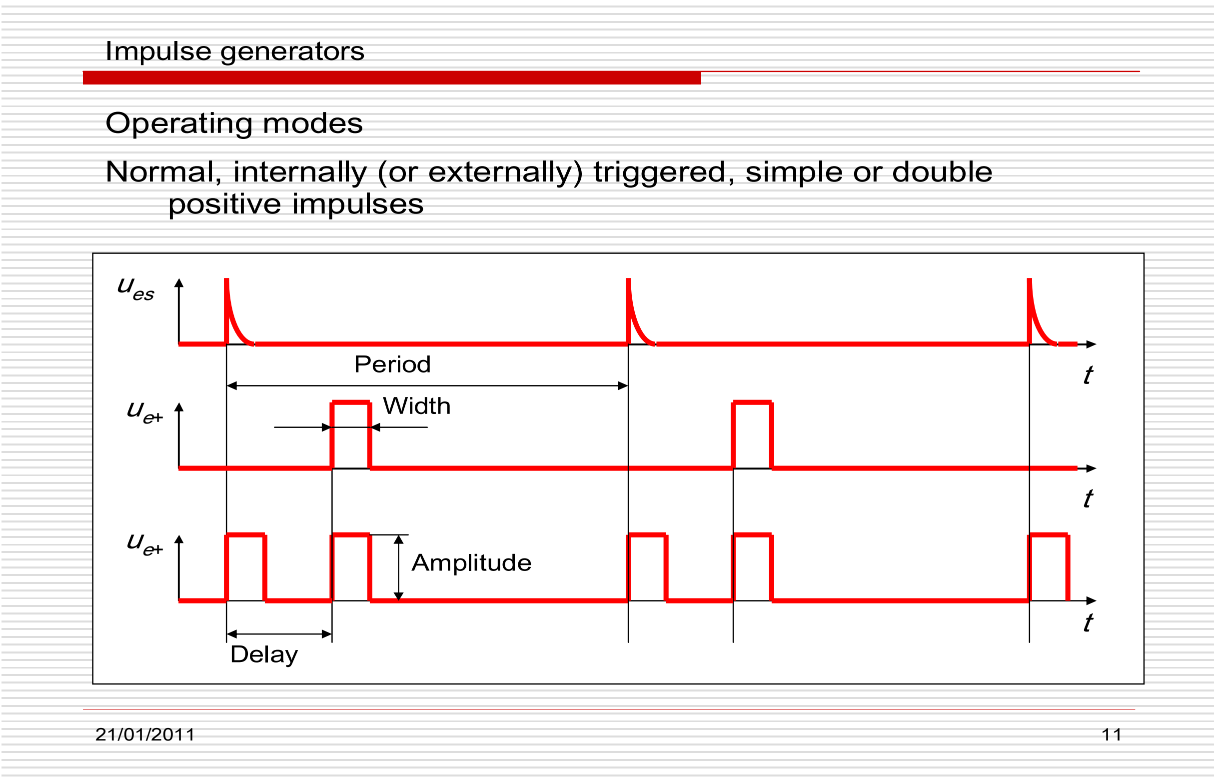
- ❑ simple or double impulses

Operating modes

Normal, internally triggered, simple positive impulses

The trigger block operates autonomously and sets the repetition rate of the generated impulses.

The generator provides, in each cycle, a trigger pulse and one pulse at each output (positive and negative), delayed with respect to the trigger pulse.

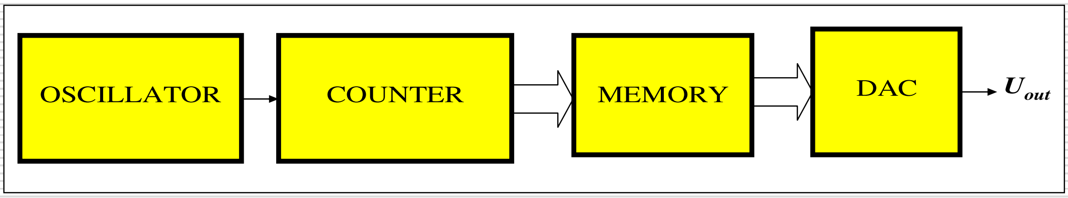


6. Signal generators. Describe the operation principle of a Direct Digital Synthesis generator.

https://intranet.etc.upt.ro/~E_INSTR/PowerPoint%20presentations%202010%202011/2%20Signal%20Generators%202010%202011.ppt, slides #35-36

Sine wave generators

Direct digital synthesis generators



Oscillator (clock generator) – frequency f_0

Counter – n bits (0 - 2^n-1) = memory address

Stored values: $\sin(2\pi i/2^n)$

Output frequency: $f_0/2^n$

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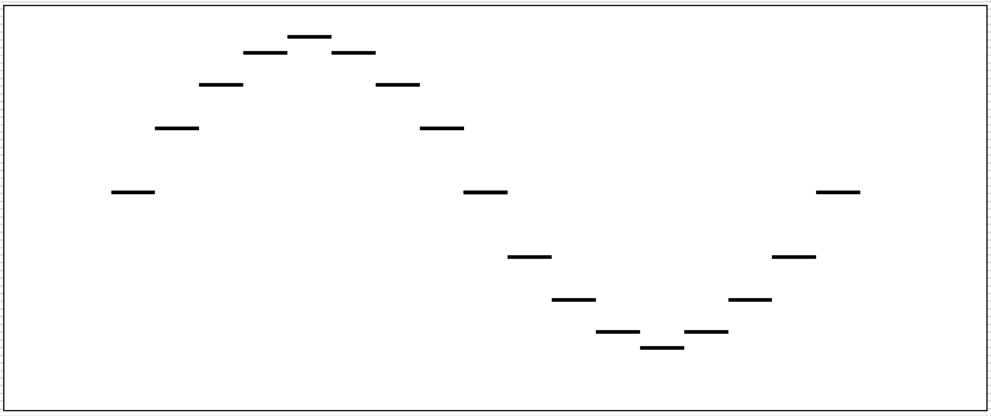
Sine wave generators

Direct digital synthesis generators - example (n=4)



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7. Digital voltmeters and multimeters. Error and data presentation rules.

https://intranet.etc.upt.ro/~E_INSTR/PowerPoint%20presentations%202010%202011/3%20Digital%20Voltmeters%20and%20Multimeters%202010%202011.ppt, slides #7-10

Introduction

The maximum permissible error

Δ_t=a% $\times$ reading + b% $\times$ range + n digits

Δ_t=a% $\times$ reading + c% $\times$ range

Δ_t=a% $\times$ reading + m digits

Remark. One digit represents one LSD.

Example. One digit is 1 mV in case of a 2 V, $3^1/_2$ digit DVM (readout x,xxx V).

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Introduction

Data presentation rules

1. Measurement error and uncertainty should be expressed with no more than two significant digits.
2. The LSD of the measurement result and of its corresponding error/uncertainty should have the same weight.

Examples.

Right	Wrong
0,2%	0,256%
3,5 mV	3,58 mV
0,02 mA	0,0222 mA

Right	Wrong
1,0 ± 0,2 mA	1 ± 0,2 mA
1,538 V ± 0,003 V	1,538 V ± 0,03 V
1,538 V ± 3 mV	1,53 V ± 3 mV

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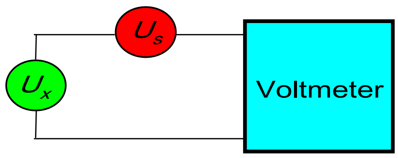
8. Digital voltmeters and multimeters. Define normal and common mode voltages and the respective rejection ratios (NMRR and CMRR)

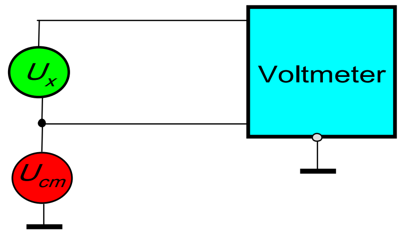
https://intranet.etc.upt.ro/~E_INSTR/PowerPoint%20presentations%202010%202011/3%20Digital%20Voltmeters%20and%20Multimeters%202010%202011.ppt, slides #20, 23, 28

DC digital voltmeters

Measurement errors due to external noise



Normal mode voltage
(DC or AC)



Common mode voltage
(DC or AC)

DC digital voltmeters

The ability of a DC DVM to reject an AC normal mode signal is described by the Normal Mode Rejection Ratio (acronym NMRR):

$$NMRR = \frac{\text{amplitude of the normal mode voltage}}{\text{equivalent DC voltage}}$$

Example. For a DC DVM with a NMRR of 100, a normal mode voltage with an amplitude of 1 V produces an additional error of

1 V/100 = 0,01 V = 10 mV.

DC digital voltmeters

The ability of a DC DVM to reject a common mode signal is described by Common Mode Rejection Ratio (acronym CMRR):

$$CMRR = \frac{\text{tensiunea perturbatoare de mod comun}}{\text{tensiunea serie echivalentă}}$$

Aplicație. Un voltmetru de tensiune continuă are CMRR = 1000. O tensiune de mod comun de 5 V conduce la o tensiune serie echivalentă de 5 V/1000 = 5 mV.

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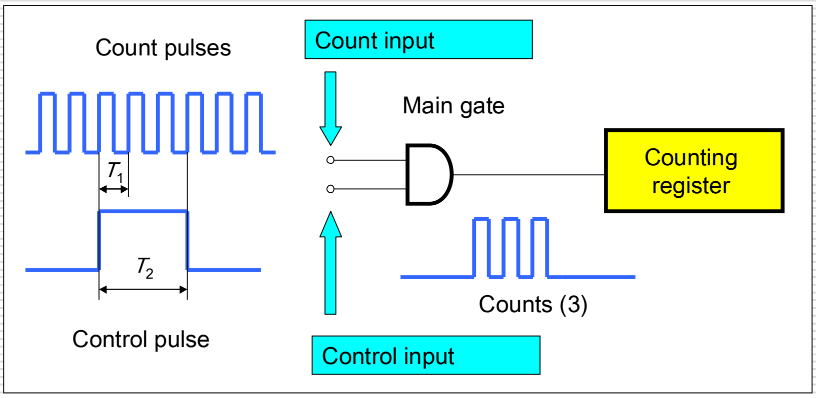
9. Universal counters. Describe the operating principle and explain how frequency can be measured.

https://intranet.etc.upt.ro/~E_INSTR/PowerPoint%20presentations%202010%202011/4%20Universal%20counters%202010%202011.ppt, slides #6-10

Universal counters

Operating principle



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Displayed result:

$$N_x = \frac{T_2}{T_1} \quad \text{or} \quad N_x = f_1 T_2$$

<u>Frequency measurement</u>

The frequency f of a repetitive signal can be defined by the number of cycles of that signal per unit of time

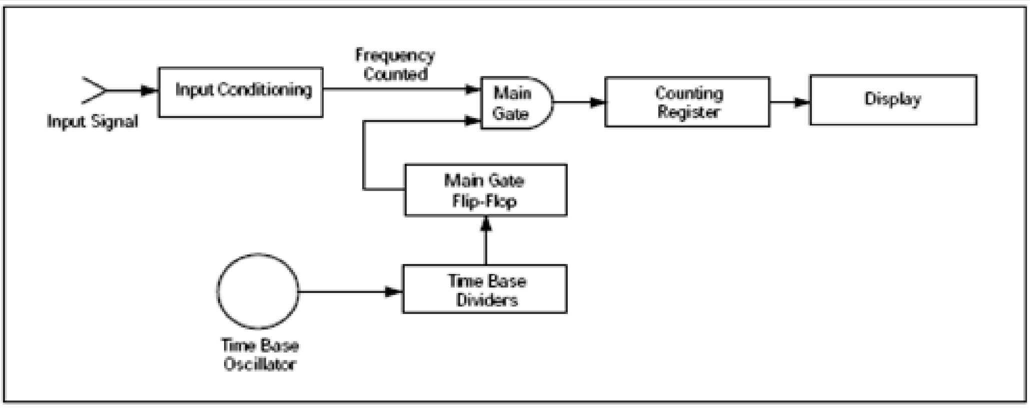
f=n/t,

where n is the number of cycles and t is the time interval in which they occur. As suggested by the above equation, the frequency can be measured by counting the number of cycles and dividing it by t. By taking t equal to one second, the number of counted cycles will represent the frequency (in Hz) of the signal.

The input signal is initially conditioned to a form that is compatible with the internal circuitry of the counter. The conditioned signal is a pulse train where each pulse corresponds to a cycle of the input signal. With the main gate open, pulses are allowed to pass through and get totalized by the counting register.

Universal counters

Basic block diagram of a universal counter in the frequency measurement mode

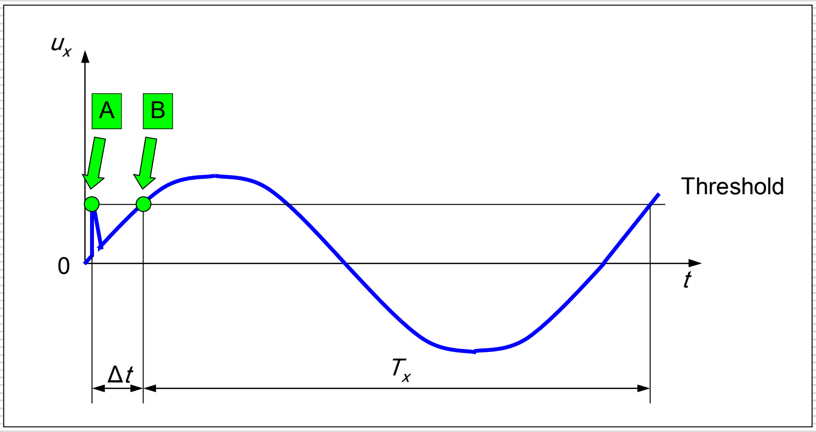


The time base oscillator together with the decade dividers and the main gate flip flop control the opening time of the main gate.

10. Universal counters. Trigger error for period measurements.

https://intranet.etc.upt.ro/~E_INSTR/PowerPoint%20presentations%202010%202011/4%20Universal%20counters%202010%202011.ppt, slides #24-26

Period measurement – trigger error



Trigger error

- for single period measurement

$$\delta_b = \frac{1}{\pi \cdot S / Z}$$

S/Z = signal to noise ratio

- for multiple period averaging

$$\delta_b = \frac{1}{N \cdot \pi \cdot S / Z}$$

Measurement uncertainty

- frequency meaurement

$$\delta_{fx\lim} = \delta_c + \delta_{osc}$$

- period measurement

$$\delta_{Tx\lim} = \delta_c + \delta_{osc} + \delta_b$$