POLITEHNICA UNIVERSITY TIMIŞOARA
Faculty of Electronics and Telecommunications
Studies in English

BACHELOR FINAL EXAM

Academic Year 2016-2017

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Core Courses

Major Courses

2nd THEMATIC AREA

MATHEMATICS – S1, S2

1. *Present Taylor's formula for functions of one variable and how can be used in approximating functions by polynomials.*

Answer:

Let $f: I \subset \mathbf{R} \to \mathbf{R}$, and $x_0 \in I$, where $f \in C^{n+1}(I)$. Then $f(x) = T_n(x) + R_n(x)$ (*Taylor's formula*),

where T_n is the Taylor's polynomial of n[th] order, and R_n is the reminder:

$$T_n(x) = f(x_0) + \frac{x - x_0}{1!} f'(x_0) + \ldots + \frac{(x - x_0)^n}{n!} f^{(n)}(x_0),$$

$$R_n(x) = \frac{(x - x_0)^{n+1}}{(n+1)!} f^{(n+1)}(x_0 + \theta(x - x_0)),\ 0 < \theta < 1.$$

It follows the approximation formula for $f(x)$ in a neighborhood V of x_0:

$$f(x) \cong T_n(x),$$

with the error $\varepsilon_n = \sup_{x \in V} |R_n(x)|$.

2. *Define the notions of eigenvalue (or proper value) and eigenvector (or proper vector) on a linear operator.*

Answer:

We consider the vector space V defined over the field **K** and the linear operator $f: V \to V$. A vector $v \in V$ (different from the null vector of V) is called an eigenvector (or proper vector) of the operator f if there exists a scalar λ from **K** such that $f(v) = \lambda v$. The scalar λ is called an eigenvalue (or proper value) of f.

3. Specify how the extremes of a function of class C^2 of two variables can be found.

Answer:

The extremes of the function $u = u(x, y)$ are among the *stationary points*, namely the solutions of the system $\begin{cases} \frac{\partial u}{\partial x} = 0 \\ \frac{\partial u}{\partial y} = 0 \end{cases}$.

A stationary point is a point of *minimum* if in this point

$$\frac{\partial^2 u}{\partial x^2} \cdot \frac{\partial^2 u}{\partial y^2} - \left(\frac{\partial^2 u}{\partial x \partial y} \right)^2 > 0 \text{ and } \frac{\partial^2 u}{\partial x^2} > 0,$$

and is a point of *maximum* if in this point

$$\frac{\partial^2 u}{\partial x^2} \cdot \frac{\partial^2 u}{\partial y^2} - \left(\frac{\partial^2 u}{\partial x \partial y} \right)^2 > 0 \text{ and } \frac{\partial^2 u}{\partial x^2} < 0.$$

4. Define the following notions: arithmetical mean, weighted arithmetical mean and geometrical mean.

Answer:

Let $\{x_1, x_2, \ldots, x_n\}$ be a non-empty set of records (real numbers) with non-negative wedges $\{p_1, p_2, \ldots, p_n\}$.

Weighted mean: $M_p = \frac{p_1 x_1 + p_2 x_2 + \cdots + p_n x_n}{p_1 + p_2 + \cdots p_n}$ (the elements with a greater weight have more contribution to the mean). We can simplify the above formula taking normalized weights $\sum_{i=1}^{n} p_i = 1$. In this case we have $M_p = \sum_{i=1}^{n} p_i x_i$

Arithmetical mean : M_a it is a particular case of the weight mean M_p when all weights are equals $p_n = \frac{1}{n}$.

We have $M_a = \frac{1}{n}\sum_{i=1}^{n} x_i = \frac{x_1 + x_2 + \cdots + x_n}{n}$ (M_a indicates the central trend of a set numbers).

Geometrical mean : $M_g = \sqrt[n]{x_1, x_2, \cdots x_n}$ if $x_i > 0$, $i = \overline{1,n}$. The geometrical mean has the following geometric explanation: the geometrical mean $M_g = \sqrt{ab}$ of two numbers a, $b \in \mathbf{R}_+$ represents the length of a square with the same area as a rectangle with lengths a and b.

5. *Define the notion of the conditional probability, write and explain the Bayes's formula.*

***Answer*:**

Let $\{E, K, P\}$ a probability space and $A, B \in K$ two events with $P(A) \neq 0$. We call the probability of the event B conditioned by the event A, the expression:

$$P_A(B) = P(B/A) = \frac{P(A \cap B)}{P(A)}$$

Let $S = \{B_1, B_2 \ldots B_n\}$ an events complete system. Therefore, $E = \bigcup_{i=1}^{n} B_i, B_i \in K, B_i \bigcap B_j = \phi, i \neq j$. We say that the system S is a partition of the sure event E, and the events B_i are called outcomes.

Bayes's formula:

$$P_A(B_i) = \frac{P(B_i) \cdot P_{B_i}(A)}{\sum_{j=1}^{n} P(B_j) \cdot P_{B_j}(A)}$$

This formula returns the probability of an outcome in the hypothesis that the event A has occured, or, more precisely, the probability that to occur the event A to be conditioned by the outcome B_i.

6. Define for a discrete (and finite) random variable the following numerical characteristics: mean value, variance and standard deviation.

***Answer*:**

Let ξ be a discrete (and finite) random variable with its probability distribution

$$\xi : \begin{pmatrix} x_1, x_2, \ldots, x_n \\ p_1, p_2, \ldots, p_n \end{pmatrix}, \sum_{i=1}^{n} p_i = 1, \; p_i = P(\xi = x_i)$$

Mean value: $M(\xi) = \sum_{i=1}^{n} x_i \; p_i$. The mean value represents a numerical value around which it's find a group of the values for this random variable.

Variance: $D^2(\xi) = \sigma^2 = M\left[(\xi - M(\xi))^2\right]$.

Standard deviation: $D(\xi) = \sigma = \sqrt{D^2(\xi)}$.

The variance and the standard deviation are indicators which explain the "scattering" of the values for a random variable, giving information on the concentration degree of the values around to its mean value.

7. Define the Laplace transform and write the formula for the derivative.

***Answer*:**

If f is an original function, then its Laplace transform is

$$(Lf)(s) = \int_0^{\infty} f(t) e^{-st} dt$$

Image of the derivative: $(Lf')(s) = s(Lf)(s) - f(0_+)$.

8. Define the Z transform (the discrete Laplace transform) and calculate its image for the unit-step signal.

***Answer*:**

If $\{fn\}$ is an original sequence, then its Z transform is:

$$Z(f_n)(z)=\sum_{n=1}^{\infty} f_n z^{-n}.$$

For the unit-step signal

$$\sigma_n=\begin{cases}0, & n<0,\\ 1, & n\geq 0,\end{cases} \qquad n\in\square$$

its Z transform is

$$Z(\sigma_n)(z)=\sum_{n=1}^{\infty} z^{-n}=\frac{1}{1-\frac{1}{z}}=\frac{z}{z-1}, \quad \text{for} \quad |z|<1.$$

9. Polar, cylindrical and spherical coordinate systems.

***Answer*:**

The conversion between the Cartesian coordinates (x, y) of a point in the plane and the polar coordinates (ρ, ϕ) of the same point is given by the relations :

$$\begin{cases}x=\rho\cos\phi\\ y=\rho\sin\phi\end{cases},$$

where $\rho \in [0, \infty)$, $\phi \in [0, 2\pi)$.

The conversion between the Cartesian coordinates (x, y, z) of a point in three-dimensional space and the cylindrical coordinates (ρ, ϕ, z) of the same point is given by the relations :

$$\begin{cases}x=\rho\cos\phi\\ y=\rho\sin\phi\\ z=z\end{cases},$$

where $\rho \in [0, \infty)$, $\phi \in [0, 2\pi)$, $z \in \mathbf{R}$.

The conversion between the Cartesian coordinates (x, y, z) of a point in three-dimensional space and the spherical coordinates (ρ, ϕ, θ) of the same point is given by the relations :

$$\begin{cases} x = \rho\cos\phi\sin\theta \\ y = \rho\sin\phi\sin\theta \\ z = \rho\cos\theta \end{cases},$$

where $\rho \in [0, \infty)$, $\phi \in [0, 2\pi)$, $\theta \in [0, \pi]$.

10. Physical and geometrical magnitudes calculated by integrals. Formula for the flux of a vector field.

***Answer*:**

Area of a plane domain, volume of a body, mass, centre of gravity, moments of inertia, the work of a field of force.

Let S be a smooth surface and let $\vec{v} = P\vec{i} + Q\vec{j} + R\vec{k}$ be a continuous vector field on S. The flux of the vector field $\vec{v}$ across the surface S oriented by the normal vector $\vec{n} = (\cos\alpha)\vec{i} + (\cos\beta)\vec{j} + (\cos\gamma)\vec{k}$ is:

$$\iint_S (\vec{v}\vec{n})dS = \iint_S (P\cos\alpha + Q\cos\beta + R\cos\gamma)dS.$$

11. Derivative with respect to a versor of a real function. Gradient, divergence and curl.

***Answer*:**

Let $f : D \subset \mathbf{R} \to \mathbf{R}$ be a scalar field, let $\vec{s} \in \mathbf{R}^3$, $\|s\|=1$, be a versor and $\vec{a} \in D$. The derivative of f in the direction of $\vec{s}$ at the point $\vec{a}$ is the limit (provided that it exists)

$$\lim_{t\to 0} \frac{1}{t}[f(\vec{a} + t\vec{s}) - f(\vec{a})] := \frac{\partial f}{\partial \vec{s}}(\vec{a})$$

The derivative $\frac{\partial f}{\partial \vec{s}}(\vec{a})$ characterizes the velocity variation of f with respect to $\vec{s}$ at the point $\vec{a}$. The gradient of f at $\vec{a}$ is defined by

$$gradf(\vec{a}) = \nabla f(\vec{a}) = \frac{\partial f}{\partial x}(\vec{a})\vec{i} + \frac{\partial f}{\partial y}(\vec{a})\vec{j} + \frac{\partial f}{\partial z}(\vec{a})\vec{k}$$

where Nabla is the operator of Hamilton: $\nabla = \frac{\partial}{\partial x}\vec{i} + \frac{\partial}{\partial y}\vec{j} + \frac{\partial}{\partial z}\vec{k}$.

It can be proved that $\frac{\partial f}{\partial \vec{s}}(\vec{a}) = \vec{s} \cdot \nabla f(\vec{a})$, that is the directional derivative of f at $\vec{a}$ in the direction $\vec{s}$ is equal to the dot product between the gradient of f and $\vec{s}$.

From here it follows that the gradient direction of a scalar field is the direction of maximum value of that field, that is the field has the fastest variation.

Let $\vec{v} : U \to \mathbf{R}$ be a vector field defined on an open set $U \subset \mathbf{R}^3$, $\vec{v} = (P, Q, R)$. The divergence of the field $\vec{v}$ at a current point is the scalar (number)

$$div\vec{v} = \frac{\partial P}{\partial x} + \frac{\partial Q}{\partial y} + \frac{\partial R}{\partial z}.$$

The curl of the field $\vec{v}$ at a current point is the vector

$$curl\vec{v} = \nabla f(\vec{a}) = \left(\frac{\partial R}{\partial y} - \frac{\partial Q}{\partial z}\right)\vec{i} + \left(\frac{\partial P}{\partial z} - \frac{\partial R}{\partial x}\right)\vec{j} + \left(\frac{\partial Q}{\partial x} - \frac{\partial P}{\partial y}\right)\vec{k}.$$

12. Write the Fourier series and the Fourier coefficients for a continuous periodic signal.

Answer: Let $f : \mathbf{R} \to \mathbf{R}$ be an integrable and periodic function having the period T and $\omega = \frac{2\pi}{T}$. The Fourier coefficients are:

$$a_n = \frac{2}{T}\int_0^T f(t)\cos(n\omega t)dt, \quad n = 0,1,...$$

$$b_n = \frac{2}{T}\int_0^T f(t)\sin(n\omega t)dt, \quad n = 1,2,...$$

The Fourier series associated to f is:

$$\frac{a_0}{2} + \sum_{n=1}^{\infty} a_n \cos(n\omega x) + b_n \sin(n\omega x).$$

13. Define the Fourier transform. The Fourier inverting formula.

***Answer*:**

The Fourier transform of an absolutely integrable function $f : \mathbf{R} \to \mathbf{C}$ is:

$$\hat{f}(\omega) = \int_R f(t)e^{-it\omega}dt.$$

The Fourier inverting formula is

$$f(t) = \frac{1}{2\pi}\int_R \hat{f}(\omega)e^{it\omega}d\omega.$$

14. Write the filtering formula and the Fourier transform for the unit impulse.

***Answer*:**

The filtering formula is: $\delta(x - x_0) = \delta_{x_0}$, where δ is the Dirac's distribution.

The Fourier transform is $\hat{\delta} = 1$.

15. Solve the Cauchy-Problem

$$\begin{cases} x'(t) = a(t)x(t) \\ x(t_0) = x_0 \end{cases}$$

where a is a continuous function.

Answer:

The given equation can be rewritten as

$$\frac{x'(s)}{x(s)} = a(s).$$

Integrating between t_0 and t, we obtain

$$\ln x(t) - \ln x(t_0) = \int_{t_0}^{t} a(s)ds \Leftrightarrow \ln \frac{x(t)}{x(t_0)} = \int_{t_0}^{t} a(s)ds.$$

Thus, the sought-for solution is

$$x(t) = x_o e^{\int_{t_0}^{t} a(s)ds} \quad .$$

1st THEMATIC AREA

PHYSICS – S3, S4, S5

1. Definition of mechanical energy

A: The general form of the definition for mechanical energy **is: E_{mech} = K + PE**
Where:
PE refers to the total potential energy of the system, including all types of potential energy; [J]
K refers to the sum of the kinetic energies of all particles in the system, [J]
E_{mech} is the total mechanic energy ; [J]

2. Definition of the kinetic energy

A: The kinetic energy ***K* of an object of mass m moving with a speed v is defined as *K* = ½ (mv^2)**
K is the kinetic energy of the moving object [J]
m is the mass of the moving object [kg]
v is the speed of the object [m/s]

3. Definition of work

A. The work ***W* done** on **a system by an** external **agent exerting a** constant force **on the system is the product of the magnitude *F* of the force, the magnitude Δr of the displacement of the point of application of the force, and cos θ,**
where θ is the angle between the force and displacement vectors. The work is a scalar quantity.
The work **is defined, mathematically, as the dot product: W =** $F \cdot \Delta r$
W is the work [J],
F **is the constant external force, vector, acting on the system [N],**
Δr **is the vector of the displacement, [m].**
The work done by a variable net force **is**

$$\sum W = W_{\text{net}} = \int \left(\sum \vec{\mathbf{F}} \right) \cdot d\vec{\mathbf{r}}$$

where the integral is calculated over the path that the particle takes through space.

4. Definition of potential energy

A: The expression of potential energy**, in linear systems, is a function of position (relative position). The corresponding force is also a function of position. Most common form of potential energy is the gravitational potential energy (some other types of potential energy are: the elastic potential energy, the magnetic potential energy, the electrostatic potential energy).**
The gravitational potential energy PE **is the energy that an object of mass *m* has by virtue of its position relative to the surface of the earth. That position is measured by the height *h* of the object relative to an arbitrary zero level:** **PE = mgh**
PE is the gravitational potential energy [J]
m is the mass [kg]
g is the gravitational acceleration [m/s^2]
h is the height [m]

5. Definition of (mechanical) power

A: Power **is the rate at which energy is expended or converted to another form. Power is connected to all types of energy and flow of energy.**

Mechanically, it is the rate at which work is done. Power is work done per unit time.

Average power: P = W/t = work[J]/time[s] .

SI Unit for power is the watt: 1W=1J/1s

6. Definition of heat

Heat is energy **that flows from a higher-temperature object to a lower-temperature object because of the difference in temperatures. The substance has internal energy, not heat. The word "**heat**" is used only when referring to the energy actually in transit from hot to cold.**

SI Unit of Heat: joule (J)

7. Conservation of mechanical energy

A: For an isolated system **the energy in the system is conserved and the sum of the kinetic and potential energies remains constant. KE + PE = constant**

The total mechanical energy**, E_{mech} = KE + PE of an object remains constant as the object moves, provided that the net work done by external nonconservative forces is zero, $W_{nc}=0$.**

8. Conservation of linear momentum (impilse) for an isolated system

A: The linear momentum **of a particle or an object that can be modeled as a particle of mass *m* moving with a velocity $\vec{v}$ is defined to be the product of the mass and velocity**: $\vec{p} = m\vec{v}$.

The total linear momentum **of an isolated (net external force equal to zero) system remains constant.**

$$\sum \vec{F} = \frac{d\bar{p}}{dt} = 0\,; \qquad \vec{p}_{tot} = \textbf{constant}$$

9. The conservation of the angular momentum

The instantaneous angular momentum **of the particle relative to the origin *O* is defined by the vector** $\bar{L}$

product of its instantaneous position vector $\bar{r}$ **and the instantaneous linear momentum** $\bar{p}$.

$$\bar{L} = \bar{r} \times \bar{p}$$

The total angular momentum **of a system is conserved if the net external torque acting on the system is zero.**

$\bar{M}_{ext} = \bar{r} \times \overline{F_{ext}}$ $\qquad$ $\bar{M} = \frac{d\bar{L}}{dt}$ $\qquad$ **External** $\bar{M} = 0\,, \rightarrow \frac{d\bar{L}}{dt} = 0\,, \rightarrow \bar{L} = \text{constant}$

10. The Hooke's law

A: The force of an elastic system (spring), inside the limits of linearity (elasticity) is given by

$$\vec{F} = -k\vec{x}$$

Where *x* is the displacement of the spring's end from its equilibrium position (a distance, in SI units: m);

***F* is the restoring force exerted by the material (in SI units: N or $kgms^{-2}$); and**

***k* is a constant called the *rate* or *spring constant* (in SI units: $N \cdot m^{-1}$ or kgs^{-2}).**

For an elastic bar: $$\Delta l = \frac{F \cdot l_0}{S \cdot E}$$

Where F is the force [N] , l_0 is the initial length of the bar [m], S is the cross section of the bar [m^2] and E is the Young' module (elasticity) of the material of the bar [N/m^2].

11. Archimede's law (principle)**:**

A: The apparent loss in weight of a body immersed in a fluid is equal to the weight of the displaced fluid

Or: a body immersed in a fluid is pushed up, in the vertical direction, with a force equal to the weight of the volume of the displaced fluid.

12. The law of absorbtion of waves

A: In a homogenous disipative media the intensity of plane waves reduces exponentially with the distance

$$I = I_0 e^{-kx}$$

where I_0 is the intensity of the penetrating wave just at the surface of the dissipative media, I is the intensity of the wave at distance x from the surface, and k is the absorption coefficient.

The absorption coefficient is a characteristic of the medium, depending also on the wave length of the incident wave

The intensity „I" of the wave is numerically equal to the energy carried by the wave in a second, trough the surface normal (orthogonal) on the wave direction of propagation.

13. The reflection laws**:**

The incident ray, the reflected ray, and the normal to the surface all lie in the same plane, and, the angle of reflection equals the angle of incidence .

14. The refraction laws**:**

When light travels from a material with refractive index n_1 into a material with refractive index n_2, the refracted ray, the incident ray, and the normal to the interface between the materials all lie in the same plane. The angle of refraction is related to the angle of incidence by $n_1 \cdot \sin\theta_1 = n_2 \cdot \sin\theta_2$.

The index of refraction *n* of a material is the ratio of the speed *c* of light in a vacuum to the speed *v* of light in the material.

15. Coulomb's law

A: The magnitude *F* of the electrostatic force exerted by one point charge q_1 on another point charge q_2 is directly proportional to the magnitudes $|q_1|$ and $|q_2|$ of the charges and inversely proportional to the square of the distance *r* between them.

$$F = \frac{q_1 \cdot q_2}{4\pi\varepsilon} \cdot \frac{1}{r^2}$$

The electrostatic force is directed along the line joining the charges, and it is attractive if the charges have unlike signs and repulsive if the charges have like signs.

3rd THEMATIC AREA

MEASURING UNITS - S6, S7, S8, S9, S10
of the International System of Units

1. Specify the SI unit and its symbol for mass. Specify the multiplier and its symbol for micro (example: atto = 10^{-18}, a).
   The SI unit for mass is the kilogram. Its symbol is kg. The multiplier for micro is 10^{-6}. Its symbol is μ.
2. Specify the SI unit and its symbol for length. Specify the multiplier and its symbol for milli (example: atto = 10^{-18}, a).
   The SI unit for length is the metre. Its symbol is m. The multiplier for milli is 10^{-3}. Its symbol is m.
3. Specify the SI unit and its symbol for time. Specify the multiplier and its symbol for micro (example: atto = 10^{-18}, a).
   The SI unit for time is the second. Its symbol is s. The multiplier for micro is 10^{-6}. Its symbol is μ.
4. Specify the SI unit and its symbol for electrical current. Specify the multiplier and its symbol for milli (example: atto = 10^{-18}, a).
   The SI unit for electrical current is the ampere. Its symbol is A. The multiplier for milli is 10^{-3}. Its symbol is m.
5. Specify the SI unit and its symbol for angular velocity. Specify the multiplier and its symbol for kilo (example: atto = 10^{-18}, a).
   The SI unit for angular velocity is the radian per second. Its symbol is rad/s. The multiplier for kilo is 10^{3}. Its symbol is k.
6. Specify the SI unit and its symbol for frequency. Specify the multiplier and its symbol for tera (example: atto = 10^{-18}, a).
   The SI unit for frequency is the hertz. Its symbol is Hz. The multiplier for tera is 10^{12}. Its symbol is T.
7. Specify the SI unit and its symbol for energy, work and heat. Specify the multiplier and its symbol for mega (example: atto = 10^{-18}, a).
   The SI unit for energy, work and heat is the joule. Its symbol is J. The multiplier for mega is 10^{6}. Its symbol is M.
8. Specify the SI unit and its symbol for power and radiant flux. Specify the multiplier and its symbol for giga (example: atto = 10^{-18}, a).
   The SI unit for power and radiant flux is the watt. Its symbol is W. The multiplier for giga is 10^{9}. Its symbol is G.
9. Specify the SI unit and its symbol for electrical charge and quantity of electricity. Specify the multiplier and its symbol for femto (example: atto = 10^{-18}, a).
   The SI unit for electrical charge and quantity of electricity is the coulomb. Its symbol is C. The multiplier for femto is 10^{-15}. Its symbol is f.
10. Specify the SI unit and its symbol for voltage, electrical potential difference and electromotive force. Specify the multiplier and its symbol for nano (example: atto = 10^{-18}, a).
    The SI unit for voltage, electrical potential difference and electromotive force is the volt. Its symbol is V. The multiplier for nano is 10^{-9}. Its symbol is n.
11. Specify the SI unit and its symbol for electrical field strength. Specify the multiplier and its symbol for mega (example: atto = 10^{-18}, a).
    The SI unit for electrical field strength is the volt per metre. Its symbol is V/m. The multiplier for mega is 10^{6}. Its symbol is M.

12. Specify the SI unit and its symbol for electric resistance, impedance and reactance. Specify the multiplier and its symbol for kilo (example: atto = 10^{-18}, a).
    The SI unit for electric resistance, impedance and reactance is the ohm. Its symbol is Ω. The multiplier for kilo is 10^{3}. Its symbol is k.
13. Specify the SI unit and its symbol for electrical conductance. Specify the multiplier and its symbol for kilo (example: atto = 10^{-18}, a).
    The SI unit for electrical conductance is the siemens. Its symbol is S. The multiplier for kilo is 10^{3}. Its symbol is k.
14. Specify the SI unit and its symbol for electric capacitance. Specify the multiplier and its symbol for pico (example: atto = 10^{-18}, a).
    The SI unit for electric capacitance is the farad. Its symbol is F. The multiplier for pico is 10^{-12}. Its symbol is p.
15. Specify the SI unit and its symbol for inductance. Specify the multiplier and its symbol for milli (example: atto = 10^{-18}, a).
    The SI unit for inductance is the henry. Its symbol is H. The multiplier for milli is 10^{-3}. Its symbol is m.

4th THEMATIC AREA

CORE COURSES – S13, S14, S15

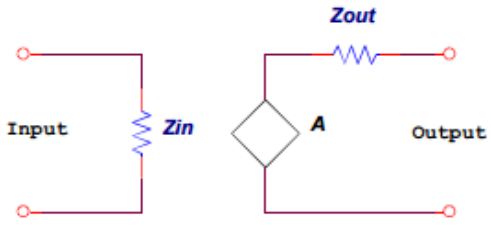
ELECTRONIC CIRCUITS

1. *Demonstrate the optimum input and output impedance for a voltage amplifier.*

2011 EC (c 01).ppt / slides 8,9

Amplifiers fundamental properties

- *Gain*
- *Input impedance*
- *Output impedance*



General amplifier model

- There are three types of gain:

voltage gain (A_V),
current gain (A_I),
power gain (A_P).

$$A_V = \frac{V_{OUT}}{V_{IN}} \qquad A_I = \frac{I_{OUT}}{I_{IN}} \qquad A_P = \frac{P_{OUT}}{P_{IN}}$$

- The gain of a circuit is determined by its component values !!!
- When the **gain** of a circuit has been calculated, it can be used to determine the **output** of the circuit for **a specified input**

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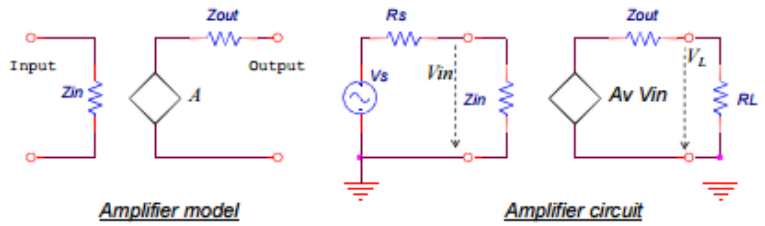
Ex: Voltage amplifier circuit



Amplifier model *Amplifier circuit*

- At the circuit input and output there are 2 voltage dividers:

$$v_{IN} = v_S \frac{Z_{IN}}{R_S + Z_{IN}} \qquad v_L = v_{OUT} \frac{R_L}{Z_{OUT} + R_L} \qquad \text{where} \quad v_{OUT} = A_V v_{IN}$$

- Since $v_{IN} < v_S$ and $v_L < v_{OUT}$

=> The *effective voltage gain* of a circuit is lower than the calculated voltage gain of the amplifier itself.

To neglect the input and output voltage drop we must have :

[Infinite gain], Infinite input impedance, Zero output impedance !!!

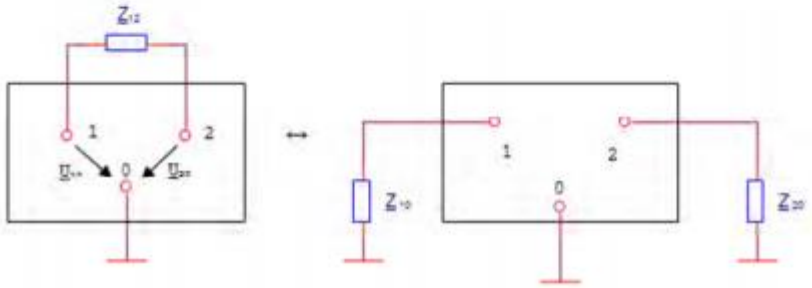
2011 Electronic Circuits | Lecture 1: Introduction to amplifiers | Slide 9

2. ***Explain Miller effect and theorem and its utility for high frequency analysis.***

2011 EC (c 03+04).ppt /slides 37-38, seminar nr.2.doc

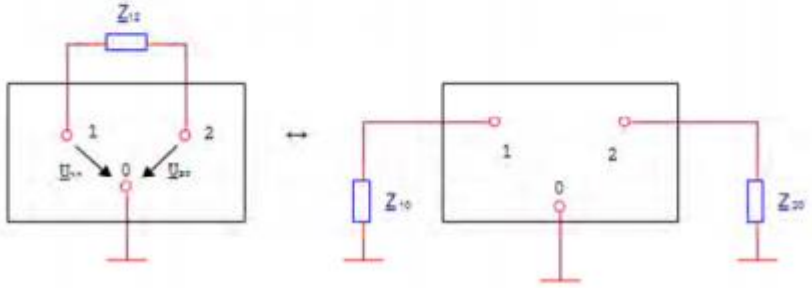
Miller Effect

An impedance Z_{12} connected from the input of an amplifier to the output can be replaced by an impedance across the input terminals (Z_{10}) and impedance across the output terminals (Z_{20}).



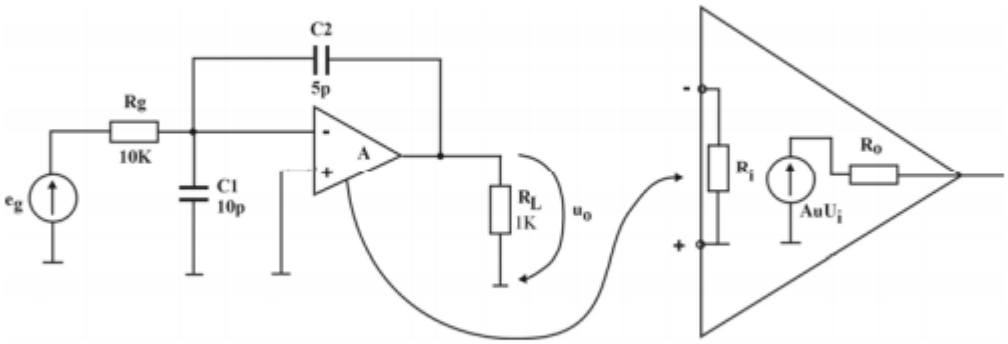
Miller Effect

An impedance Z_{12} connected from the input of an amplifier to the output can be replaced by an impedance across the input terminals (Z_{10}) and impedance across the output terminals (Z_{20}).



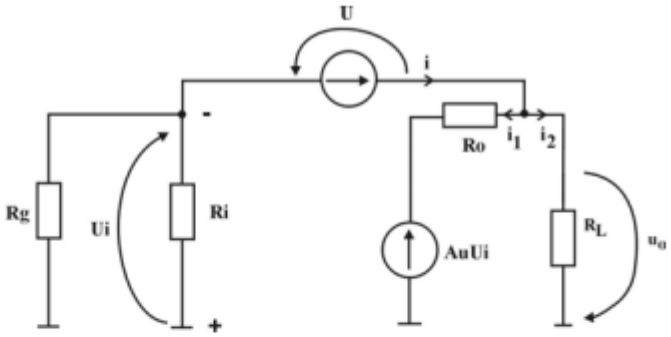
Example: For the following circuit, we consider the amplifier's parameters:

$A_u = 10^2$, $R_i = 1M\Omega$, $R_0 = 1K$.



Compute high cut of limit frequency of the circuit, using Miller's theorem

Answer:



$$f_{p_1} = \frac{1}{2\pi(C_{10} + C_1)R_g \| R_i} = 60KHz \quad f_{p_2} = \frac{1}{2\pi(C_{20})R_g \| R_i} = 64KHz$$

$$C_{10} = C_2(1-K),\ C_{20} = C_2(1-\frac{1}{K}),\ K = \frac{U_o}{U_i} = \frac{A_u U_i \dfrac{R_L}{R_o + R_L}}{U_i} = A_u \frac{R_L}{R_o + R_L}$$

$f_{p2} >> f_{p1} \rightarrow$ $\qquad f_i \cong f_{p1} = 60\text{KHz}$

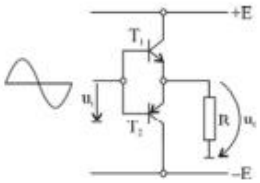
3. *Which amplifier class is known for its crossover distortions? Explain the root cause and ways of improvement based on a simplified schematic and is transfer characteristic.*

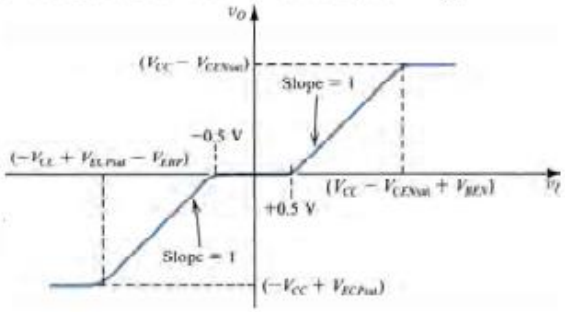
2011 EC (c 05).ppt / slides 22-24, 37

Class B - output stage circuit

Named also *Complementary-symmetry amplifier*

= 2 complementary BJT's used as emitter followers, working in "push pull" mode.





Advantage: good efficiency – up to 78.5% (in DC mode – no current sink from supply)

Drawback: Crossover distortion

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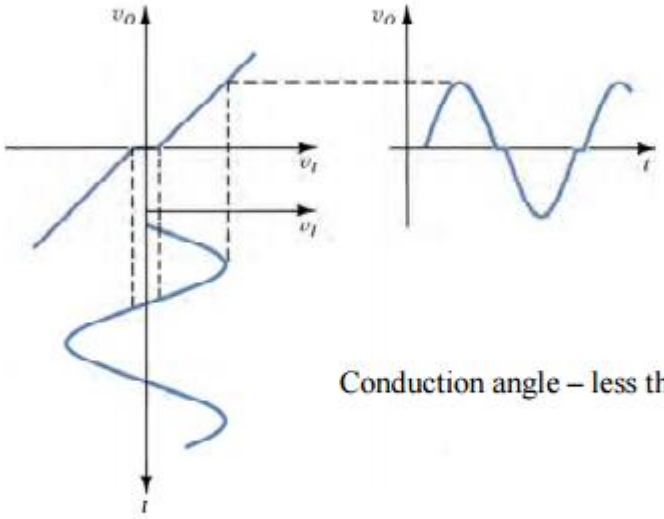
Class B – crossover distortion

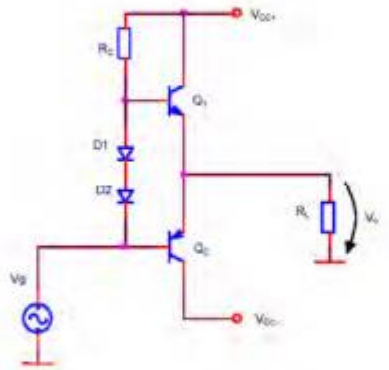


Conduction angle – less than ½ T

=> crossover distortion between the "halves" of the signal

Class B biasing

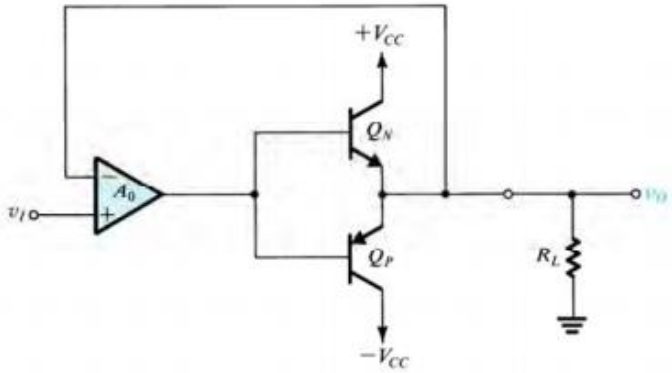
Biasing must provide V(B1)- V(B2) to keep Q1 and Q2 off, but close to conduction => lower crossover distortion



BJT 's can be biased using 2 diodes or a "V_{BE} multiplier" circuit => constant voltage drop between Q1 and Q2 bases

Opamp Implementation

Op amp connected in a negative-feedback loop to reduce crossover distortion



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4. *Describe half bridge class D amplifiers topology, block schematic and principle of operation.*

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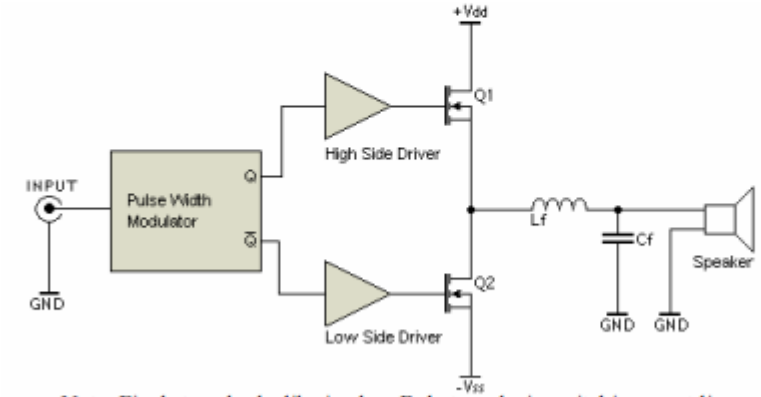
Class D – (half bridge) simplified circuit

– operation is switching, hence the term *switching power amplifier*
– output devices are rapidly switched on and off at least twice for each cycle
– the output devices are either completely on or completely off so theoretically they do not dissipate any power



Note: Final stage looks like in class B, but works in switching – not linear mode !!!

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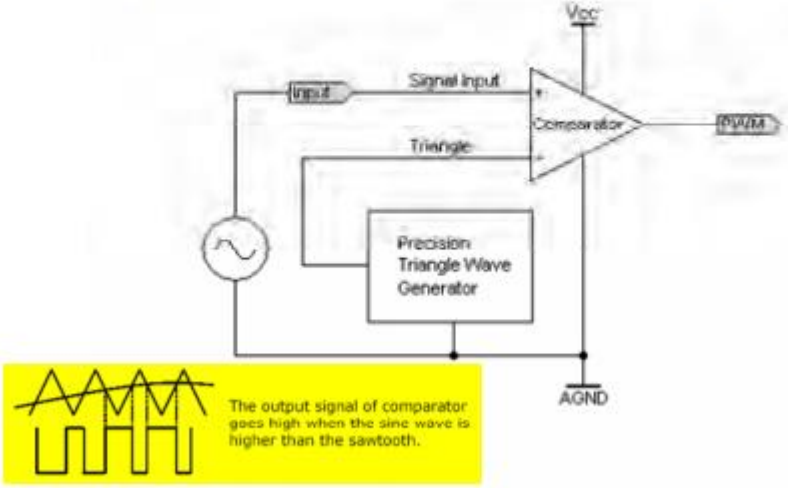
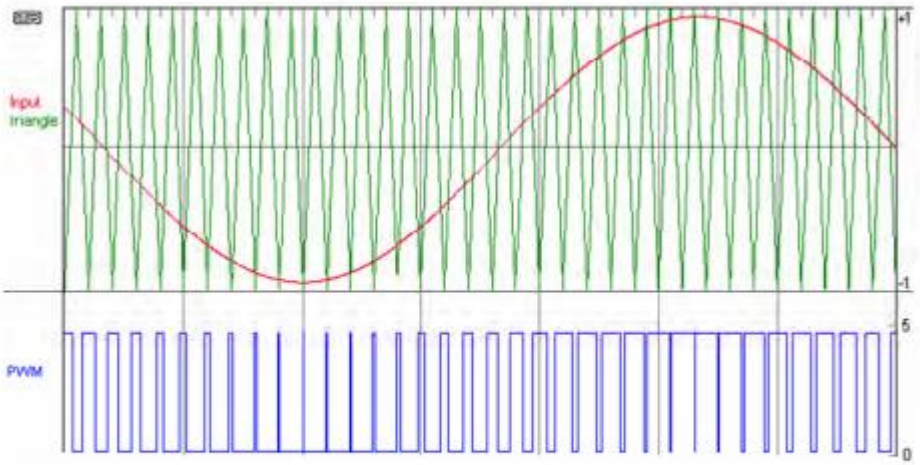
Class D - PWM signal generation

- The input signal is compared with a triangle signal resulting in a PWM (Pulse width modulation) signal



Class D – PWM waveforms



- Usually 150KHz to 250Khz switching freq. is used
- The LC LPF provide at the output the mean value of the PWM signal - same shape as the Input signal

5. *Using formula show the most unwanted occurrence place for an external perturbation in a multistage amplifier sing a gobal negative feedback loop*

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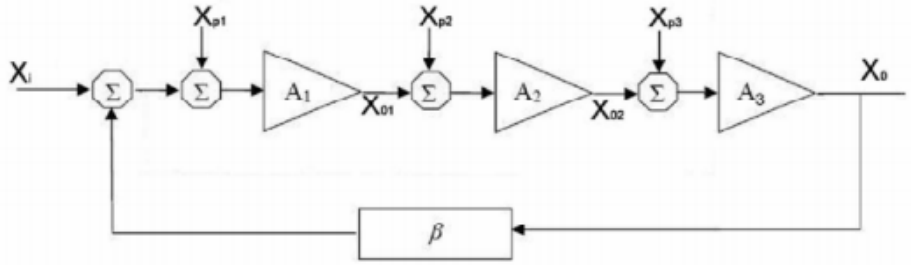
Perturbation influence in Feedback Amps



$$\begin{cases} x_0 = (x_{02} + x_{p3})A_3 \\ x_{02} = (x_{01} + x_{p2})A_2 \\ x_0 = (x_\Sigma + x_{p1})A_1 \\ x_\Sigma = x_i - x_r = x_i - \beta x_0 \end{cases}$$

Perturbations are reduced as they are closer to output

$$x_0 = (((x_i - \beta x_0 + x_{p1})A_1 + x_{p2})A_2 + x_{p3})A_3$$

$$\Rightarrow x_0 = x_i \frac{A_1A_2A_3}{1+\beta A_1A_2A_3} + x_{p1}\frac{A_1A_2A_3}{1+\beta A_1A_2A_3} + x_{p2}\frac{A_2A_3}{1+\beta A_1A_2A_3} + x_{p3}\frac{A_3}{1+\beta A_1A_2A_3}$$

6. *Demonstrate bandwidth extension for an amplifier when a negative feedback is applied.*

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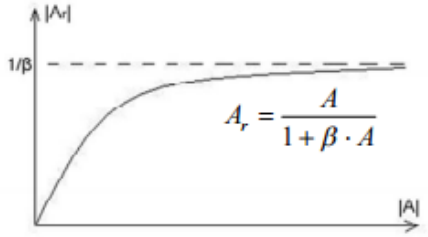
Feedback effect over gain

- For amplifiers with feedback we can assume that the



$A_r = \dfrac{A}{1+\beta \cdot A}$

If nonfeedback amplifier has : $\Delta A / A$

$\Delta A_r / A_r \overset{???}{\longleftrightarrow} \Delta A / A$

At small variations :

$$\Delta A_r \cong \frac{1+\beta A - A\beta}{(1+\beta A)^2} \cdot \Delta A = \frac{1}{(1+\beta A)^2} \cdot \Delta A = \frac{A}{1+\beta A} \cdot \frac{1}{1+\beta A} \cdot \frac{\Delta A}{A} \Rightarrow$$

$$\frac{\Delta A_r}{A_r} \cong \frac{\Delta A}{A} \cdot \frac{1}{1+\beta A} = \frac{\Delta A}{A} \cdot \frac{1}{F}$$

F times improvement !!!

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Influence of the feedback on freq. response

If $A(j\omega) = \dfrac{P(j\omega)}{Q(j\omega)} \cdot A_0$ and $\beta = \beta_0$ a real number,

Then: $A_r(j\omega) = \dfrac{\dfrac{P}{Q} \cdot A_0}{1+\beta_0 \dfrac{P}{Q} \cdot A_0} = \dfrac{PA_0}{Q+\beta_0 PA_0}$

only the poles are shifted

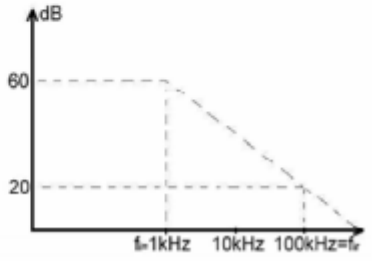
Influence of the feedback on freq. response(@high freq.)

$$\text{EX 1}: A(j\omega) = \frac{A_0}{1 + j\frac{f}{f_i}} \qquad \beta = \beta_0$$

$$A_r(j\omega) = \frac{\frac{A_0}{1 + j\frac{f}{f_i}}}{1 + \frac{\beta_0 A_0}{1 + j\frac{f}{f_i}}} = \frac{A_0}{1 + \beta_0 A_0 + j\frac{f}{f_i}} = \frac{A_0}{1 + \beta_0 A_0} \cdot \frac{1}{1 + j\frac{f}{f_i(1 + \beta_0 A_0)}} = A_{r0} \cdot \frac{1}{1 + j\frac{f}{f_{ir}}}$$

where $A_{r0} = \frac{A_0}{1 + \beta_0 A_0}$ & $f_{ir} = f_i(1 + \beta_0 A_0)$

Then: $A_r = \frac{A}{F}$; $f_{ir} = f_i F$; $A_r \cdot f_{ir} = A \cdot f_i$



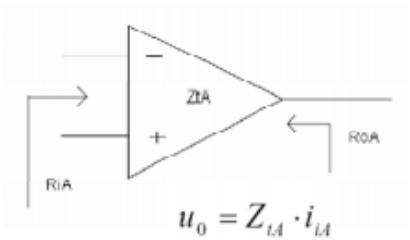
Note: only if circuit still behave linear !!!

7. *Show input and output resistance change for an amplifier when a shunt-shunt feedback is applied. Justify with formulas.*

2011 EC (c 08).ppt / slides 7,8,10

Shunt Shunt Negative Feedback

$$\begin{cases} u_0 = Z_t \cdot \dfrac{R_L \| R_{if}}{R_L \| R_{if} + R_0} \cdot i_i \\ i_i = i_{iA} \cdot \dfrac{R_g \| R_{of}}{R_g \| R_{of} + R_i} \\ i_{iA} = i_g - i_r = i_g - \beta u_0 \end{cases}$$



$$u_0 = Z_{tA} \cdot i_{iA}$$

$$Z_{tA} = \frac{u_0}{i_g}\Big|_{\beta=0}$$

$$\beta = \frac{i_r}{u_0}\Big|_{u_i=0}$$

-Obtained by separating feedback network

$$u_0 = \underbrace{Z_t \cdot \frac{R_L \| R_{if}}{R_L \| R_{if} + R_0} \cdot \frac{R_g \| R_{of}}{R_g \| R_{of} + R_i}}_{Z_{tA}} \cdot i_{iA}$$

Z_{tA}

Transfer impedance of the amp. with influences included and no feedback

Shunt Shunt Negative Feedback

$$Z_{iA} = Z_{ir}\,|\;_{i_g=0}$$

$$u_0 = Z_{iA}\cdot i_{iA} = Z_{iA}(i_g - i_r) = Z_{iA}(i_g - \beta u_0)$$

$$\Rightarrow \quad \boxed{Z_{ir} = \frac{u_0}{i_g} = \frac{Z_{iA}}{1+\beta\cdot Z_{iA}}}$$

$$R_{ir} = \frac{u_i}{i_g}$$

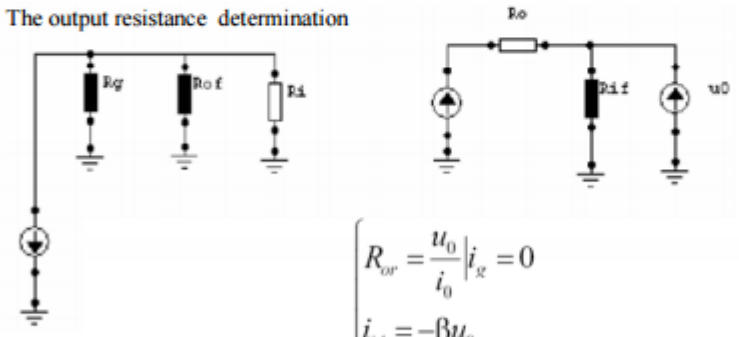
$$i_g = i_r + i_{iA} = \beta u_0 + \underbrace{\frac{u_i}{R_g \| R_{of} \| R_i}}_{R_{iA}} = \beta u_0 + \frac{u_i}{R_{iA}} = \beta\cdot Z_{iA}\cdot i_{iA} + \frac{u_i}{R_{iA}}$$

$$i_g = \beta\cdot Z_{iA}\cdot\frac{u_i}{R_{iA}} + \frac{u_i}{R_{iA}} \quad \Rightarrow \quad \boxed{R_{ir} = \frac{u_i}{i_g} = \frac{R_{iA}}{1+\beta\cdot Z_{iA}}}$$

Small value, because ig split also to the feedback network.

Shunt Shunt Negative Feedback

The output resistance determination



$$R_{or} = \frac{u_0}{i_0}\,|\;i_g=0$$

$$\begin{cases} R_{or} = \dfrac{u_0}{i_0}\Big|_{i_g=0} \\ i_{iA} = -\beta u_0 \\ i_0 = \dfrac{u_0}{R_{if}} + \dfrac{u_0 - Z_f\cdot i_i}{R_0} \Rightarrow i_0 = \dfrac{u_0}{R_{if}} + \dfrac{u_0(1+\beta Z_f)}{R_0} \\ i_i = i_{iA}\cdot\dfrac{R_g\|R_{of}}{R_g\|R_{of}+R_i} \end{cases}$$

8. *Draw noise equivalent schematic of an amplifier and define noise factor F.*

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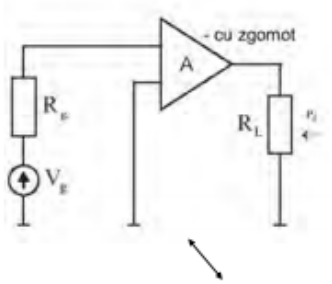
Noise model for an Amplifier

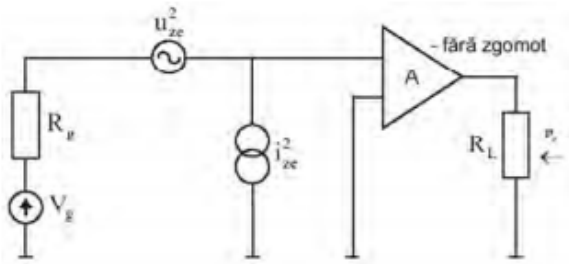


If the noise sources are uncorrelated, noise at output:

$$P_z = \sum_{k=1}^{n} P_{zk}$$

$$P_{zk} \rightarrow i_{zk}^2, u_{zk}^2 \rightarrow R_L$$

$u_{zet}^2 = u_{ze}^2 + i_{ze}^2 \cdot R_g^2$ Total noise voltage



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Noise figure (factor)

- Compare noise produced by the amp. with the noise produced by the generator Rg

$$F = \frac{SNR_{in}}{SNR_{out}}$$ SNR – signal to noise ratio

$$F \overset{def}{=} \frac{\text{Puterea totală de zgomot de la ieșire}}{\text{Puterea de zgomot datorată generatorului}}$$

$$F_{dB} = 10 \lg F$$

$$F_{dB} = 10 \lg \frac{P_{zg} + P_{zA}}{P_{zg}} \text{ unde } P_{zg} = \frac{u_{zg}^2}{(R_g + R_i)^2} \cdot R_i^2$$

$$P_{zA} = \frac{u_{ze}^2}{(R_g + R_i)^2} \cdot R_i^2 + \frac{i_{ze}^2 \cdot R_g^2}{(R_g + R_i)^2} \cdot R_i^2$$

$$F_{dB} = 10 \lg \left(1 + \frac{u_{ze}^2 + i_{ze}^2 \cdot R_g^2}{u_{zR_g}^2} \right) \qquad u_{zR_g}^2 = 4kTR_g \cdot \Delta f$$

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9. *Explain dominant pole (lag) compensation method. How is related dominant pole frequency to gain unity frequency f_{0dB}. Show practical implementation.*

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4.1 Dominant-pole compensation

It represents a very popular method, also called **lag compensation**. It consists in adding another pole in the open-loop transfer function - A(jω) - at a very low frequency, such that the loop-gain drops to unity by the time the phase reaches -180°:

$$A_C(j\omega) = A(j\omega)\frac{1}{1+j\dfrac{f}{f_d}}$$

$$f_d << \min(f_{pk})$$

where f_{pk} are the pole frequencies for A(jω).

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A serious disadvantage of this compensation method is the resulting close-loop amplifier bandwidth, drastically reduced (fig. 4).

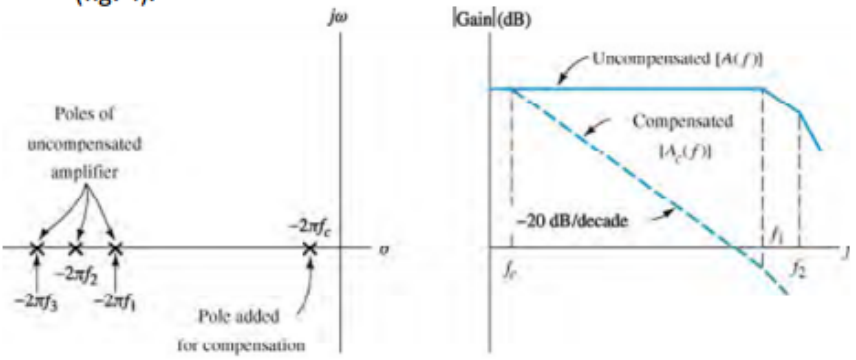

Fig. 4. Dominant-pole compensation.

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It could be shown that knowing f_{0dB} is sufficient for computing f_d:

$$f_d = f_{0dB}\left|\frac{A_f}{A_0}\right|$$

where A_0 is the open-loop midband frequency gain.

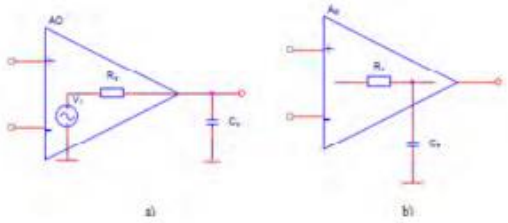


Fig. 5. Dominant-pole implementation.

10. Draw and characterize a Wien network and show how is connected to build a Wien oscillator. What are the conditions used to design feedback loops.

2011 EC (c 12,13).ppt / slides 18,11,19
2011 Sem 7.ppt

3.2 The Wien Bridge Oscillator

An oscillator circuit in which a balanced bridge is used as the feedback network

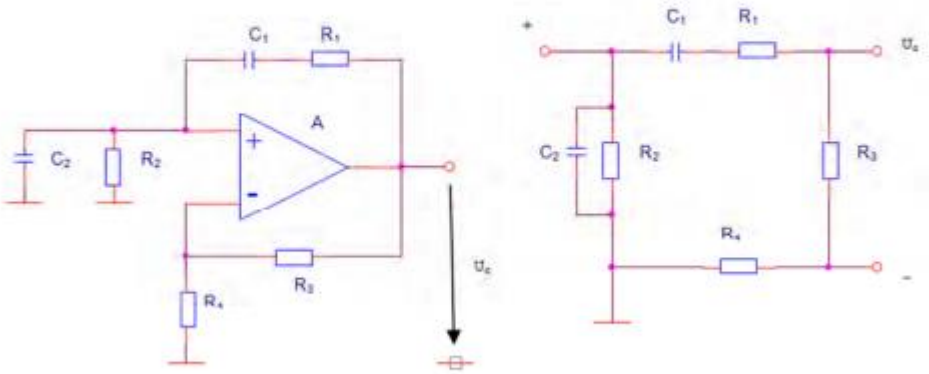


Fig. 4. a) A Wien bridge oscillator. b) The bridge network

- The condition for the feedback loop to provide sinusoidal oscillation of frequency ω is:

$$A(j\omega)\beta(j\omega) = 1 \Leftrightarrow$$

$$\begin{cases} \arg A(j\omega) + \arg \beta(j\omega) = 2k\pi & \text{phase criterion} \\ |A(j\omega)||\beta(j\omega)| = 1 & \text{amplitude criterion.} \end{cases}$$

Amplitude criterion. $$|\underline{A}_{ur}||\underline{\beta}_+|_{\omega=\omega_0} = 1$$

For negative feedback loop: $$\underline{A}_{ur} = \frac{A_u}{1+\beta_- A_u} \cong \frac{1}{\beta_-}$$

=> $$|\underline{\beta}_+| = |\underline{\beta}_-|$$

$$\beta_- = \frac{R_4}{R_3 + R_4}$$

$$\beta_+(j\omega) = \frac{1}{1 + \frac{R_1}{R_2} + \frac{C_2}{C_1} + j\left(\omega C_2 R_1 - \frac{1}{\omega C_1 R_2}\right)}$$

In order to obtain oscillations, **phase criterion** has to be satisfied:

$$\beta_+(j\omega_0) \in \Re \Rightarrow \omega_0 C_2 R_1 - \frac{1}{\omega_0 C_1 R_2} = 0;$$

$$\omega_0^2 = \frac{1}{R_1 C_1 R_2 C_2} \Rightarrow f_0 = \frac{\omega_0}{2\pi} = \frac{1}{2\pi\sqrt{R_1 C_1 R_2 C_2}}$$

$$\begin{cases} \arg[\beta_+(j\omega_0)] = 0 \\ |\beta_+(j\omega_0)| = \dfrac{1}{1 + \dfrac{R_1}{R_2} + \dfrac{C_2}{C_1}} \end{cases}$$

1. Explain how a decoder can be used as a demultiplexer.

Any binary decoder with an enable input can be used as a demultiplexer. The decoder's enable input is connected to the data line and its select inputs determine which of the output lines is driven with the data bit. The following example shows how 74HC(T)138 can be used as demultiplexer.

If the decoder's enable input active HIGH ("1") is connected to the data line and the select inputs are A=C="1" and B="0" at the output Y5 one can find the data bit negated. The remaining output lines are "1" (see Fig.1.1.)

If the decoder's enable input active LOW ("0") is connected to the data line and the select inputs are A=C="1" and B="0" at the output Y5 one can find the data bit. The remaining output lines are "1" (see Fig.1.2.)

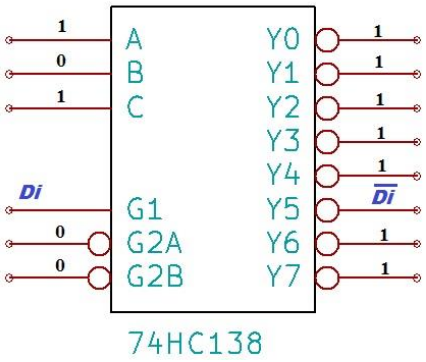


Fig. 1.1

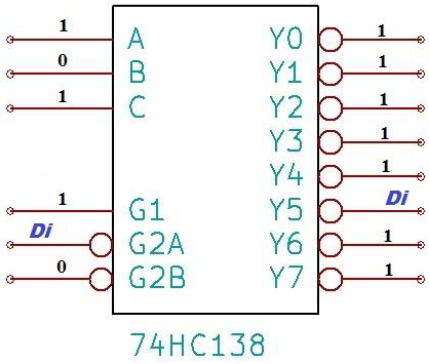


Fig. 1.2

2. Positive edge triggered D type flip-flop: draw a symbolic representation, the truth table and its associated waveforms

One of the simplest flip-flops which is produced on the market is the Positive – edge – triggered D flip-flop. This samples its D input and changes it's Q and $\overline{Q}$ outputs only on the rising edge of a controlling CLK signal (see Fig.

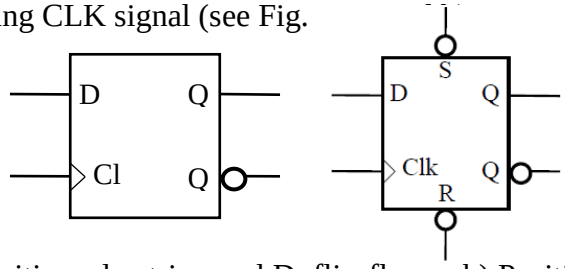


Fig. 2.1 a) Positive edge triggered D flip-flop b) Positive edge triggered D flip-flop with asynchronous inputs.

Table 1. Truth table for the D flip-flop

D	CLK	Q
1	↑ **edge**	1
0	↑ **edge**	0
X	**0**	Last Q
X	**1**	Last Q

The edge-triggered D flip-flop has a setup and hold time window during which the D inputs must not change. This window occurs around the triggering edge of CLK, and is indicated by shaded color Fig 2.2.

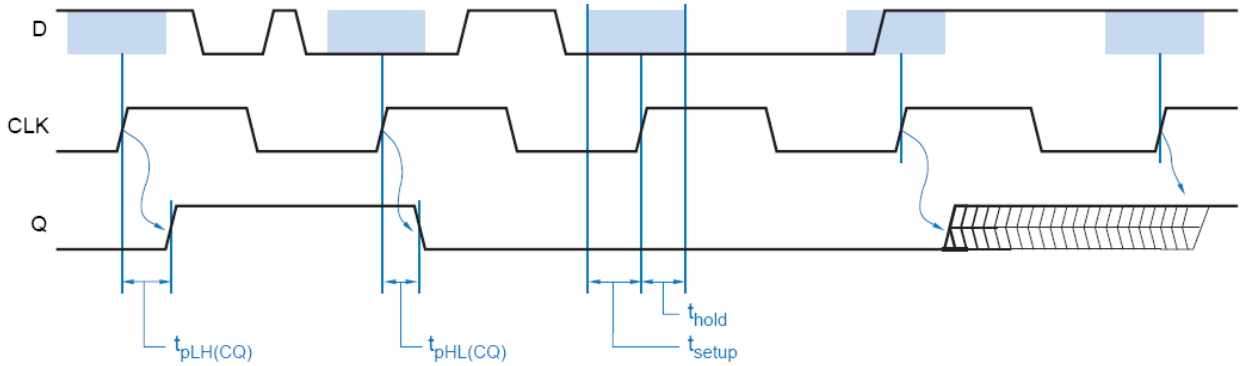


Fig. 2.2 Positive edge triggered D flip-flop waveforms

Some D flip-flops have *asynchronous inputs* (see Fig. 2.1. b) that may be used to force the flip-flop to a particular state independent of the CLK and D inputs, they are best reserved for initialization and testing purposes, to force a sequential circuit into a known starting state. If the asynchronous inputs are active LOW and S=”0” and R=”1” the output Q is “1”, no matter what logic value is at the D input. If R=”0” and S=”1” the output is Q is “0”, no matter what logic value is at the D input.

3. T (Toggle) flip-flop: draw a symbolic representation, the truth table and its associated waveforms

A *T (toggle) flip-flop* changes state on every tick of the clock (T=”1”). Such a flip-flop can be obtained from a JK-MS flip-flop by connecting its J and K inputs together.

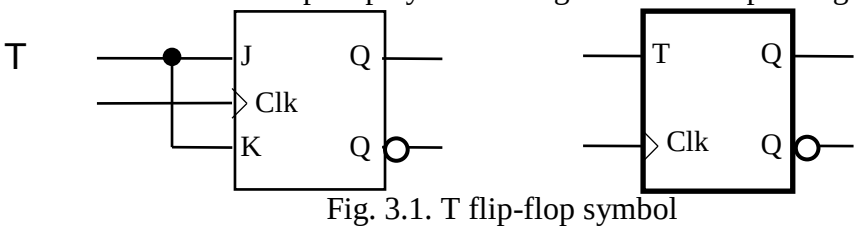


Fig. 3.1. T flip-flop symbol

Table 3.1. Truth table for a T flip-flop

T	Q_{n+1}
0	Q_n
1	$\overline{Q}_n$

Notice that the signal on the flip-flop's Q output has precisely half the frequency of the CLK input (see Fig. 3.2).

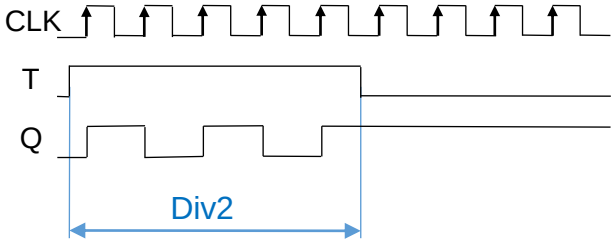


Fig. 3.2 Positive edge triggered T flip-flop waveforms

4. Explain how Serial – Parallel and Parallel – Serial conversion can be implemented with shift registers.

Serial – Parallel conversion is implemented with a SIPO register, in order to perform the conversion *n* ticks of a clock signal that corespond to the *n* bits of the binary word are needed.

Let's consider an eight bit SIPO register, the serial sequence of information clocked into the register is D_7, D_6, ... D_0. The register is cleared by connecting the */CLR* to "0". After 8 ticks of the clock signal, D_7 (the MSB) can be found at the output Q_7 and the word is held by the register an can be read out as a 8-bit value.

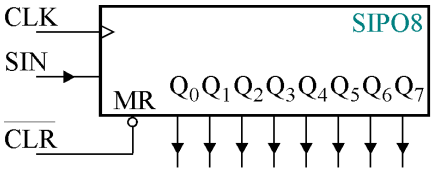


Fig 4.1 SIPO register for Serial-Paralel conversion

A proper timing should exist between the CLK and the SIN.

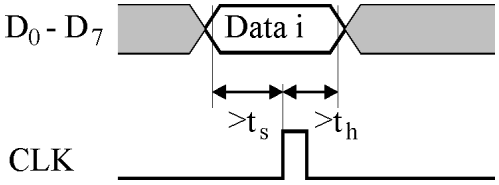


Fig 4.2 Proper timing between the CLK and the SIN (setup and hold time must be respected)

For the serial sequence of information 10101101:

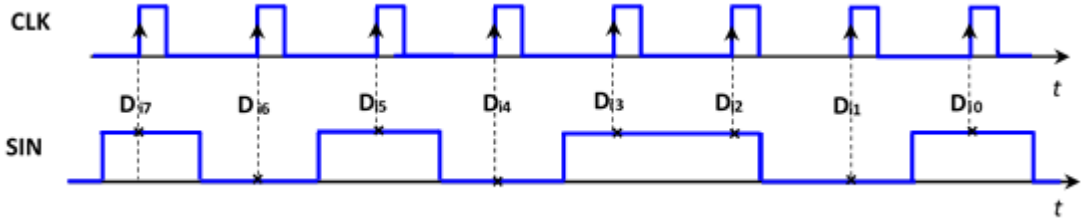


Fig 4.3 Proper timing between the CLK and the SIN an example

Parallel – Serial conversion is implemented with a PISO register. In order to perform the conversion *n* ticks of a clock signal that corespond to the *n* bits of the binary word are needed (one for loading the data and n-1 for reading it).
First the SH/nLD input is connected to "0" logic. The transfer of the input data takes place when the clock signal transitions from low to high. In order to read the data the input SH/nLD = "1", and in n-1 ticks of the clock signal the data is read out.

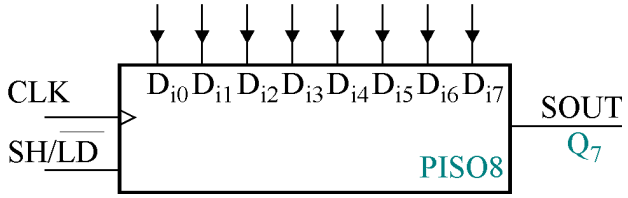


Fig 4.4 PISO register for Paralel- Serial conversion

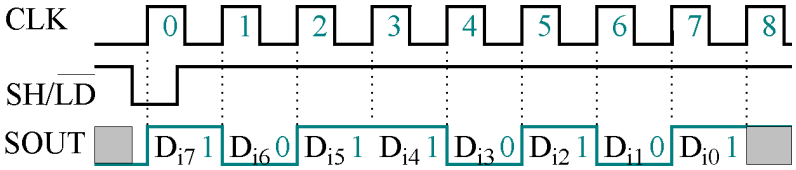


Fig 4.5 Waveforms for the serialoutput.

5. Sequential access memories FIFO and LIFO

A sequential memory is a memory in which the stored data cannot be read or written in random order, but must be addressed in a specific sequence. There are two main ways of organizing a sequential memory—as a **queue** or as a **stack**.

A queue is a **first-in first-out** (**FIFO**) memory, meaning that the data can be read only in the same order they are written. This memory can be implemented using SISO shift registers which can shift the data to the right.

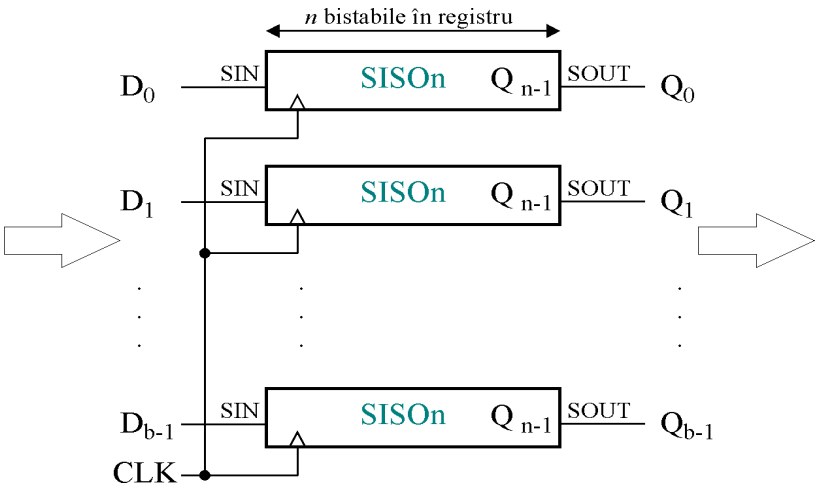


Fig. 5.1 Sequential memory

The binary words on *b* bit are written in parallel to the *b* serial inputs by applying a clock tick and shifting the data to the right. Once the words are written in the registers the first word to be read is the first one loaded in the memory. Once the data is read it is lost.

One common use for FIFO memory is to connect two devices that have different data rates. For instance, a computer can send data to a printer much faster than the printer can use it. To keep the computer from either waiting for the printer to print everything or periodically interrupting the computer's operation to continue the print task, data can be sent in a burst to a FIFO, where the printer can read them as needed.

The **last-in-first-out** (LIFO), or stack, is based on the following operation principle: the last bit to be written is the first bit to be read. This memory can be implemented using SISO shift registers which can shift the data bidirectional. To write the data the same principle from FIFO is used. To read the content of the memory, the data is shifted to the left.

The LIFO memory can be used for the storage of data that are to be retrieved in reverse order. Most microprocessors use a stack to save status flag bits and the contents of certain registers, in case of interruptions.

6. 4-bit Up Binary Ripple Counter: draw the schematic, explain how it works, and draw the relevant waveforms

A 4-bit up binary ripple counter build with 4 T flip-flops (from JK-MS with T ="1") can be seen in Fig 5. The clock ticks are applied only to the first flip-flop. The next flip-flops have as clock signal the output Q of the previous flip-flop (MR – Master Reset is synonym to R – Reset or CLR - Clear).

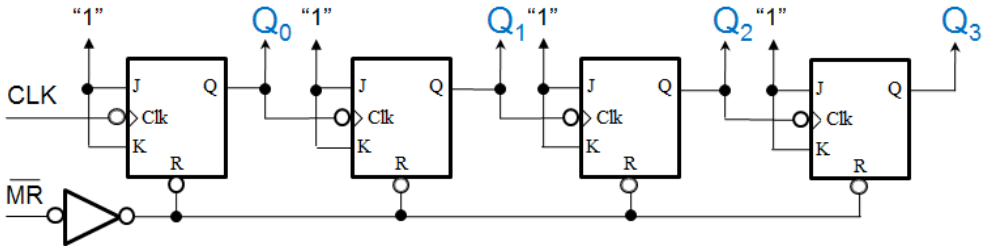


Fig 6.1. 4-bit Up Binary Ripple Counter

Clk tick	Q_3	Q_2	Q_1	Q_0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0

Observations:

1) The counter counts up, at each CLK tick the value of the counter is incremented with one unit.

2) The counter is modulus 16 (it has 4 flip-flops), the 16th tick of the clock close the cycle and brings the counter to zero. The 17th tick of the clock is the first tick from the next cycle.

3) At a certain moment of time, the binary code read at the outputs, corresponds to the number of ticks from that cycle (after 11 ticks $Q_3Q_2Q_1Q_0$ = 1011 this corresponds to number 11 coded in binary). This is practically the counting function.

4) The flip-flops works as frequency dividers by 2. The output Q_0 divides by 2 the clock signal, Q_1 divides by 2 the frequency of the signal Q_0 and by 4 the clock signal and so on.

5) In order to extend the modulus of the counter multiple counters can be cascade (the output Q_3 is connected to the CLK input of the next counter).

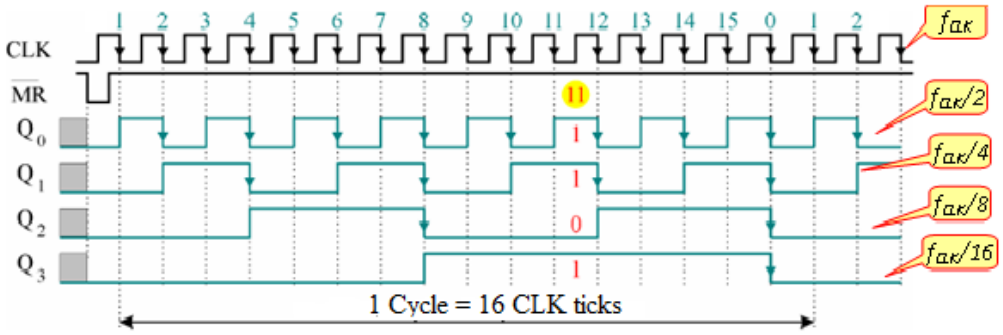


Fig 6.4. 4-bit Up Binary Ripple Counter waveforms

In order to get a countdown counter, the output $\overline{Q}$ of the flip-flop is connected to the CLK input of the next flip-flop.

7. 4 bit synchronous counter: draw the schematic, explain how it works

A *synchronous counter* connects all of its flip-flop clock inputs to the same common CLK signal, so that all of the flip-flop outputs change at the same time, after only t_{TQ} ns of delay. The main advantage of synchronous counters is their capability to count at higher clock frequency (35 MHz typically).

11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

According to the state of the counter some flip-flops have to toggle while others not. As shown in Fig.7.1, this requires the use of T flip-flops with the T input available; the output of the flip-flop toggles on the falling edge of the CLK if and only if T is asserted ("1" logic). Additional logic circuits are needed to generate the correct value for the T inputs according to its truth table.

Looking at the table one can notice that Q_0 has to toggle at each tick of the clock so $T_0 = 1$;

- Q_1 toggles only if $Q_0 = 1$ before the new tick of the clock, so $T_1 = Q_0$;
- Q_2 toggles if Q_0 and Q_1 are „1", so $T_2 = Q_0 \cdot Q_1 = Q_1 \cdot T_1$
- Q_3 toggles if Q_0, Q_1 and Q_2 are „1", so $T_3 = Q_0 \cdot Q_1 \cdot Q_2 = Q_2 \cdot T_2$.

The general rule is: $T_{n-1} = Q_0 \cdot Q_1 \cdot \ldots \cdot Q_{n-2} = T_{n-2} \cdot Q_{n-2}$.

The T values can be generated using 2 methods:

- ***Serial*** –the current value of T is obtained from the previous ones:

$$T_2 = T_1 \cdot Q_1 \quad \text{and} \quad T_3 = T_2 \cdot Q_2 .$$

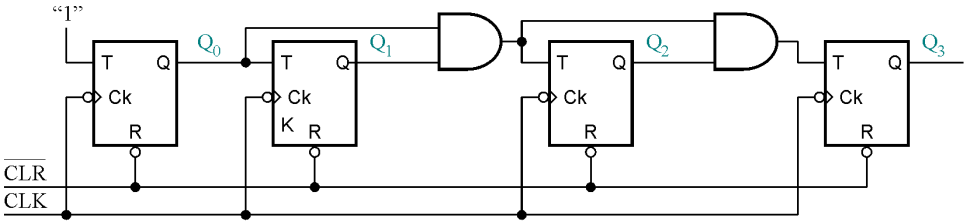


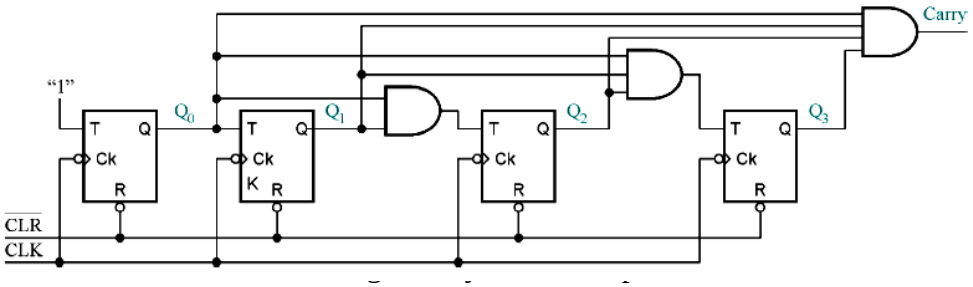
Fig. 7.1 Synchronous serial counter

$$T_{CLK\ \min} = t_{PCLK \to Q} + (n-2)t_{PAND} + \Delta t$$

Disadvantage: t_p greater that the t_p value obtain using the parallel method.
Advantage: only AND gate with 2 inputs are needed.

- ***Parallel*** – the T values are obtain from the Q values :

$$T_2 = Q_0 \cdot Q_1 \text{ and } T_3 = Q_0 \cdot Q_1 \cdot Q_2$$



$$T_{CLK\ \min} = t_{PCLK \to Q} + t_{PSI} + \Delta t$$

The t_p value is smaller, so the operating frequency is grater compared to a serial synchrounous counter. The Carry signal is obtained from Q_0, Q_1, Q_2, şi Q_3.

$Cy = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3$ and is applied at the T input of the next flip-fop when the counters are cascaded.

8. Present the main methods used to implement Programmable Frequency Dividers

Version 1 – with count down counter and parallel load

This is the most common method of obtaining a programmable ferquecy divider. It is based on the use of a reversible (count down) counter with parallel load. The number used to performe division (k) is loaded using the parallel inputs by activating /LD. The counter is decremented by the frequency f_{CLK} applied at the Count Down (Dn) until reaches the state 0000. At this moment the output Borrow (/ Bo) goes to "0" logic and enables the input /LD, and a new load of the counter with k number is performed.

Since the flip-flops used to build the counter do not have the same loading time and thus there is a risk of incomplete load, an SR flip-flop to store the charge pulse it is needed (the same as for modulo p counters). Thus, at the output /Q its yield f_{CLK}/k.

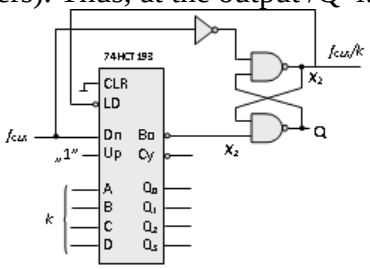


Fig 8.1 Programmable Frequency Divider with parallel load

Version 2 – with count up counter and comparator

The method uses an asynchronous counter (4040) and two 4-bit comparators (74LS85) which specifies the division ratio k. The counter conts up from 0 to a value set by the switches k [KPD1 and KPD2]. When the counter riches the preset values the comparators detects the equality and activates the clear signal /MR. In this example is an 8-bit design.

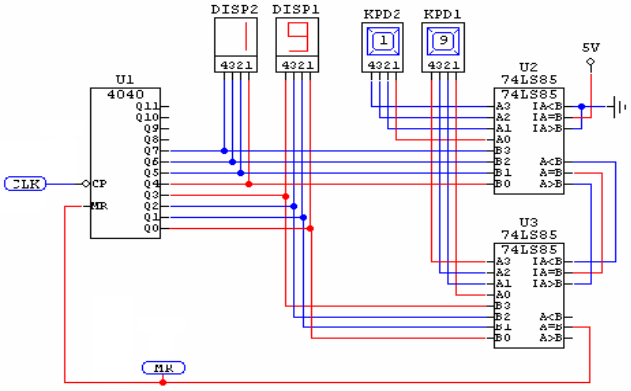


Fig 8.2 Programmable Frequency Divider with comparators

To obtain a 12-bit frequency divider a 12-bit counter and a 12-bit comparator are needed.The schematic shown above works very well in digital simulation, but not in practical implementation because CMOS and TTL LS circuits are used togheter. To solve this shortcoming, it is best to use HC or HCT circuits: 74HCT4040 and 74HCT85, in this case the design will not present any shortcoming.

Version 3 – with count up/down counter

It uses 4029 counters with paralel load controled by a NOR gate which has the number of inputs equal to the number of 4029 circuits that are use.

The circuit offers:

- count up from the preset number k to 255
- count down, from k to 0 (if $U/\overline{D}=0$)
- binary counting (if $B/\overline{D}=1$);
- decimal counting (if $B/\overline{D}=0$).

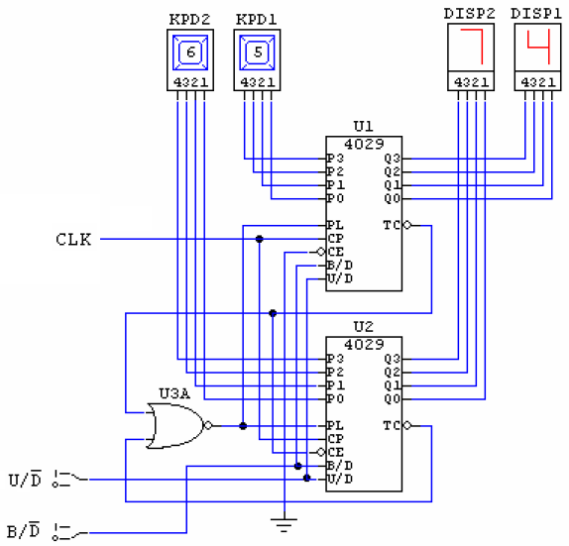


Fig 8.3 Programmable Frequency Divider with count up/down counter and OR gate

9. Shift Register Counters – Johnson Counter

A shift register can be combined with combinational logic to form a state machine whose state diagram is cyclic.

Such a circuit is called a *shift-register counter*. Unlike a binary counter, a shift-register counter does not count in an ascending or descending binary sequence, but it is useful in many "control" applications nonetheless.

An n-bit shift register with the complement of the serial output fed back into the serial input is a counter with 2*n* states and is called a twisted-ring, **Moebius**, or **Johnson** counter.

The block diagram and the waveforms for a 4 bit Johnson counter are shown below. The decoded outputs are **glitch free**.

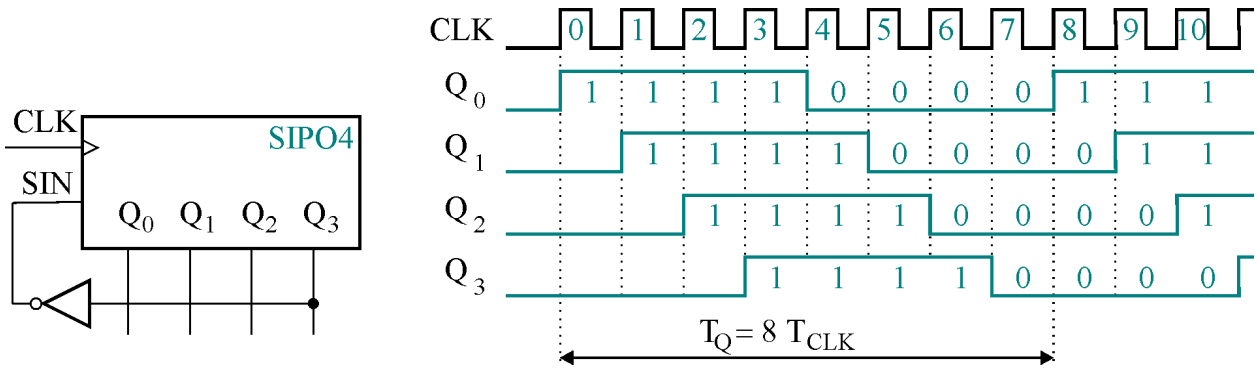


Fig. 9.1 Block diagram and the waveforms for a 4 bit Johnson counter

Table 9.1 The truth table of a 4 bit Johnson counter

CLK	Q_0	Q_1	Q_2	Q_3	
	0	0	0	0	$\overline{MR}$ =0
0	**1**	0	0	0	$\overline{MR}$ =1
1	**1**	**1**	0	0	
2	**1**	**1**	**1**	**0**	
3	**1**	**1**	**1**	**1**	
4	0	**1**	**1**	**1**	
5	0	0	**1**	**1**	
6	0	0	0	**1**	
7	0	0	0	0	
8(0)	**1**	0	0	0	
9(1)	**1**	**1**	0	0	
10(2)	**1**	**1**	**1**	0	

10. Present the main advantages and disadvantages of SRAM memories compared to DRAM memories

The tow RAM categories are:

SRAM – Static Random Access Memory - where the basic (store) cell is a D latch, the technology used is Bipolar transistors, NMOS or CMOS;

DRAM – Dynamic Random Access Memory - where the basic (store) cell is a capacitor, the technology used is NMOS or CMOS.

SRAM memory keeps data for an unlimited time, until it is rewritten. In contrast, DRAM requires constant rewriting (refreshing) -once a few millisecond- of the data, otherwise the information is lost.

SRAM advantages: high utility due to the operation mode and very high speed (access time ratio SRAM / DRAM = 8-16).

SRAM disadvantages: lower integration density and a much higher price than a DRAM memory (capacity typically ratio DRAM / SRAM = 4-8 and the ratio of cost SRAM / DRAM = 8-16).

1. CC-CE, CC-CC and Darlington configurations – draw the schematics for these configurations and name the main parameters most often used to characterize these circuits. pg. 204, course #2

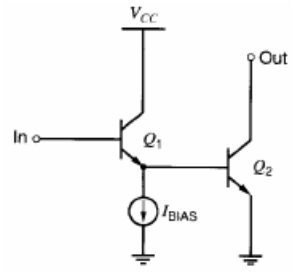


Fig. 1.

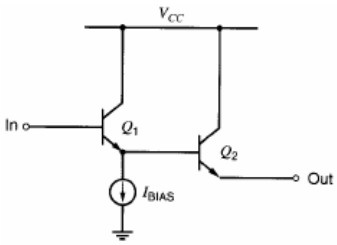


Fig. 2.

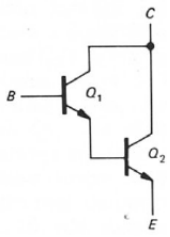


Fig. 3.

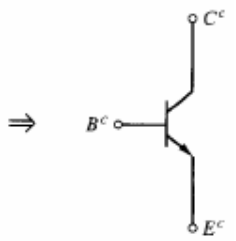


Fig.4.

(Abstract: These configuratios increase the input resistance and the current gain; the V_{BE} is twice the normal and the saturation voltage is at least V_{BE}.)

The common-collector - common-emitter (CC-CE), common-collector-common-collector (CC-CC), and Darlington configurations are all closely related. They incorporate an additional transistor to boost the current gain and input resistance of the basic bipolar transistor. The common-collector-common-emitter configuration is shown in Fig. 1. The biasing current source I_{BIAS} is present to establish the quiescent dc operating current in the emitter-follower transistor Ql**;** this current source may be absent in some cases or may be replaced by a resistor. The common-collector-common-collector configuration is illustrated in Fig. 2. In both of these configurations, the effect of transistor Q_l is to increase the current gain through the stage and to increase the input resistance.

The Darlington configuration, illustrated in Fig. 3, is a composite two-transistor device in which the collectors are tied together and the emitter of the first device drives the base of the second. A biasing element of some sort is used to control the emitter current of Ql**.** The result is a three-terminal composite transistor that can be used in place of a single transistor in common-emitter, common-base, and common-collector configurations. The term *Darlington* is often used to refer to both the CC-CE and CC-CC connections.

For the purpose of the low-frequency, small-signal analysis of circuits, the two transistors Q_l and Q_2 can be thought of as a single composite transistor, as illustrated in Fig. 4. The composite transistor has much higher input resistance and current gain than a single transistor.

r_π^c is the resistance seen looking into the composite base BC with the composite emitter EC grounded (Fig 5):

$$r_\pi^c = r_{\pi 1} + (\beta_0 + 1) r_{\pi 2}$$

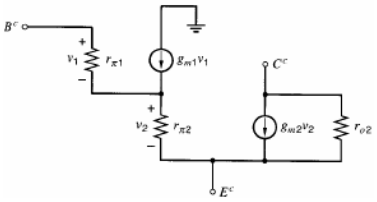


Fig. 5.

For the special case in which the biasing current source I_{BIAS} is zero, the effective current gain β^c is the ratio:

$$\beta^c = \frac{i_c^c}{i_b^c} = \frac{i_{c2}}{i_{b1}}; = \frac{\beta_0 i_{b2}}{i_{b1}} = \frac{\beta_0 i_{e1}}{i_{b1}} = \frac{\beta_0 (\beta_0 + 1) i_{b1}}{i_{b1}} = \beta_0 (\beta_0 + 1)$$

The base-emitter drop is twice normal; the saturation voltage is at least one diode drop. The combination tends to act like a slow transistor; this is taken care of by including a

resistor, R (few hundres Ohms – power transistor or a few thousend Ohms – small-signal Darlington).

2. The bipolar cascode configuration – draw the circuit, compare its output resistance with that of the common emitter stage. pg. 207, course #2

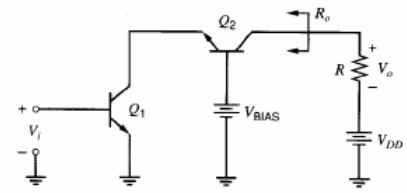


Fig. 6

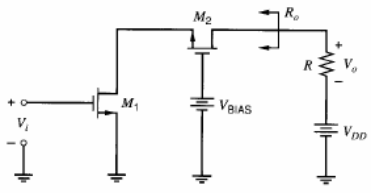


Fig. 7.

(Abstract: The cascode connection displays an output resistance that is larger by a factor of about β_0 than the CE stage alone.)

The cascode configuration is important mostly because it increases output resistance and reduces unwanted capacitive feedback in amplifiers, allowing operation at higher frequencies than would otherwise be possible. The high output resistance attainable is particularly useful in desensitizing bias references from variations in power-supply voltage and in achieving large amounts of voltage gain.

In bipolar form, the cascode is a common-emitter-common-base (CE-CB) amplifier, as shown in Fig. 6. The MOS version is shown in Fig. 7.The small-signal equivalent for the bipolar cascode circuit is shown in Fig. 8. The output resistance can be calculated by shorting the input v_i to ground and applying a test signal at the output. Then $v_1 = 0$ and the g_{mv1} generator is inactive (Fig. 9).

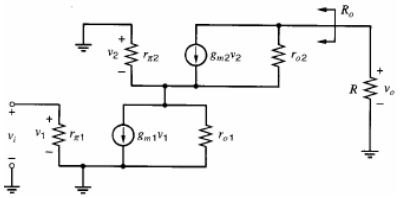


Fig. 8.

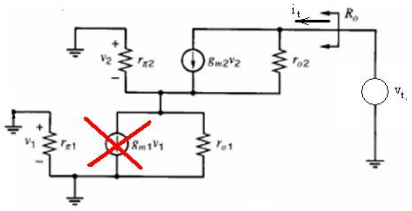


Fig. 9.

$$v_2 = -i_t\left(r_{\pi 2}\|r_{o1}\right) \qquad i_2 = i_t - g_{m2}v_2 = i_t\left[1 + g_{m2}\left(r_{\pi 2}\|r_{o1}\right)\right] \qquad v_t = -v_2 + i_2 \cdot r_{o2}$$

$$\Rightarrow R_o = \frac{v_t}{i_t} = r_{\pi 2}\|r_{o1} + r_{o2} + r_{o2}g_{m2}\cdot\left(r_{\pi 2}\|r_{o1}\right) \cong$$

$$\cong r_{o2}\left[1 + g_{m2}\cdot\left(r_{\pi 2}\|r_{o1}\right)\right] = r_{o2}\left[1 + g_{m2}\cdot\left(\frac{r_{\pi 2}r_{o1}}{r_{\pi 2} + r_{o1}}\right)\right] = r_{o2}\left(1 + \frac{g_{m2}r_{o1}}{1 + \frac{g_{m2}r_{o1}}{\beta_0}}\right)$$

If $g_{m2}r_{o1} >> \beta_0$ and $\beta_0 >> 1$ than $R_o \cong \beta_0 r_{o2}$

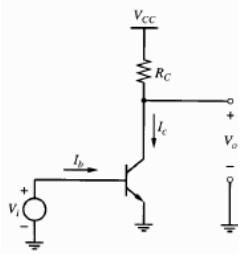


Fig. 10.

The cascode connection displays an output resistance that is larger by a factor of about β_0 than the CE stage alone (shown in Fig. 10) (we assumed that R_C is very large and can be neglected).

3. The dc transfer characteristic of an emitter-coupled pair - compare the schemes with and without emitter degeneration. We know the values for collector currents:

$$I_{c1} = \frac{\alpha_F I_{TAIL}}{1+\exp\left(-\frac{V_{id}}{V_T}\right)}; \qquad I_{c2} = \frac{\alpha_F I_{TAIL}}{1+\exp\left(\frac{V_{id}}{V_T}\right)}$$

pg. 215 – 217(abstract), course#2.

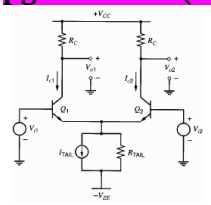


Fig. 11.

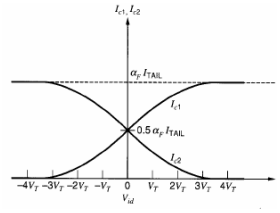


Fig. 12.

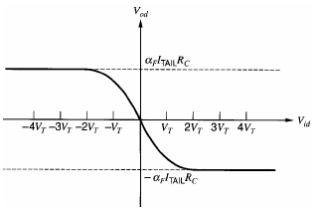


Fig. 13.

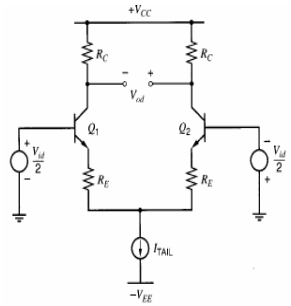


Fig. 14.

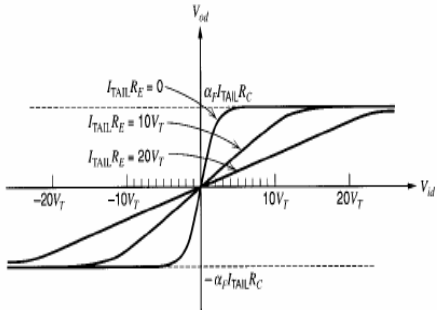


Fig. 15.

(Abstract: The circuit behaves in a linear fashion only when the magnitude of v_{id} is less than about V_T. The property „for v_{id}=0 we have v_{od}=0" allows direct coupling of cascaded stages. To increase the range of v_{id} emitter-degeneration resistors are included.)

The simplest form of an emitter-coupled pair is shown in Fig. 11. The large-signal behavior of the emitter-coupled pair is important in part because it **illustrates the limited range of input voltages over which the circuit behaves almost linearly.** These two currents are shown as a function of V_{id} in Fig. 12. When the magnitude of V_{id} is greater than about $3V_T$, the collector currents are almost independent of V_{id} because one of the transistors turns off and the other conducts all the current that flows. Furthermore, the circuit behaves in an approximately linear fashion only when the magnitude of V_{id} is less than about V_T . We can now compute the output voltages as: $V_{o1} = V_{cc} - I_{c1}R_C$; $V_{o2} = V_{cc} - I_{c2}R_C$

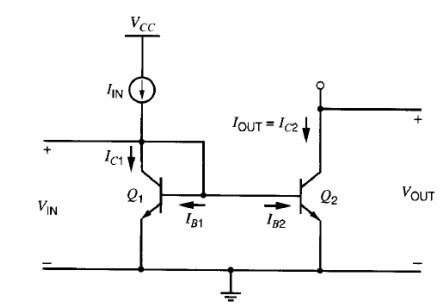
The output signal of interest is often the difference between V_{o1} and V_{o2}, which we define as V_{od}. Then:

$$V_{od} = V_{o1} - V_{o2} = \alpha_F I_{TAIL} R_C \tanh\left(\frac{-V_{id}}{2V_T}\right)$$

This function is plotted in Fig. 13. Here a significant advantage of differential amplifiers is apparent: when V_{id} is zero, V_{od} is zero if Q_1 and Q_2 are identical and if identical resistors are connected to the collectors of Q_l and Q_2. This property allows direct coupling of cascaded stages without offsets.

To increase the range of V_{id} over which the emitter-coupled pair behaves approximately as a linear amplifier, emitter-degeneration resistors are frequently included, as shown in Fig.14. The effect of the resistors may be understood intuitively from the examples plotted in Fig. 15. For large values of emitter-degeneration resistors, the linear range of operation is extended by an amount approximately equal to I_{TAIL} R_E. Furthermore, since the voltage gain is the slope of the transfer characteristic, the voltage gain is reduced by approximately the same factor that the input range is increased.

4. Simple current mirror - bipolar version. Draw the schematic and compare it with an ideal current mirror. pg. 256, course #4



(Abstract : The output current for a simple current mirror must exactly mirror the input current but, in a real circuit, I_{OUT} is less then the input current, I_{IN}. Ideally: the output current is equal to the input current, independent of V_{OUT}, with V_{IN} = 0. A current mirror must provide a constant current at the output and an infinity output resistance.)
Fig. 16.

Ideally: the output current is equal to the input current multiplied by a desired current gain (if the gain is unity - **current mirror**); the current-mirrors gain is independent of input frequency; the output current is independent of the voltage between the output and common terminals; the voltage between the input and common terminals is ideally zero because this condition allows the entire supply voltage to appear across the input current source; more than one input and/or output terminals are sometimes used.

The simplest form of a current mirror consists of two transistors. Fig. 16 shows a bipolar version of this mirror. Transistor Q1 is diode connected, forcing its collector-base voltage to zero. In this mode, Q_1 operates in the forward-active region. Assume that Q_2 also operates in the forward-active region and that both transistors have infinite output resistance. Then I_{OUT} is controlled by $V_{BE2} = V_{BE1}$ (KVL).

$$V_{BE2} = V_T \ln \frac{I_{C2}}{I_{S2}} = V_{BE1} = V_T \ln \frac{I_{C1}}{I_{S1}}$$

$$\Rightarrow I_{C2} = \frac{I_{S2}}{I_{S1}} I_{C1} \quad \text{and if} \quad I_{S1} = I_{S2} \quad \text{shows that} \quad I_{C1} = I_{C2}$$

$$I_{IN} - I_{C1} - \frac{I_{C1}}{\beta_F} - \frac{I_{C2}}{\beta_F} = 0 \qquad I_{OUT} = I_{C2} = I_{C1} = \frac{I_{IN}}{1 + \frac{2}{\beta_F}}$$

In practice, the devices need not be identical.

$$\Rightarrow I_{C2} = \frac{I_{S2}}{I_{S1}} I_{C1} = \left(\frac{I_{S2}}{I_{S1}} I_{IN} \right) \left(\frac{1}{1 + \frac{1 + (I_{S2}/I_{S1})}{\beta_F}} \right)$$

At the input:

$$V_{IN} = V_{CE1} = V_{BE1} = V_{BE(on)}$$

Since $V_{BE(on)}$ is proportional to the natural logarithm of the collector current, V_{IN} changes little with changes in bias current.
The minimum output voltage required to keep Q_2 in the forward-active region is:

$$V_{OUT(min)} = V_{CE2(sat)}$$

5. Wilson current mirror – draw the schematic of the bipolar version, estimate the value of the output resistance and compare it with that of the cascode current mirror pg. 277, Course#6

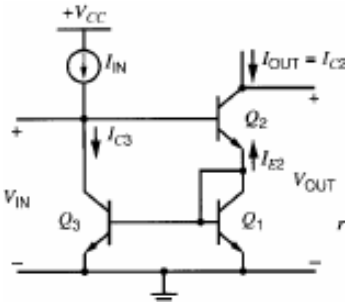


Fig. 17.

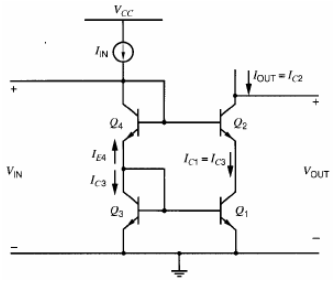


Fig. 18.

(Abstract: Both circuits, the Wilson current mirror and the cascode current mirror achieve a very high output resistance: $R_o \approx \frac{\beta_0 r_{o2}}{2}$)

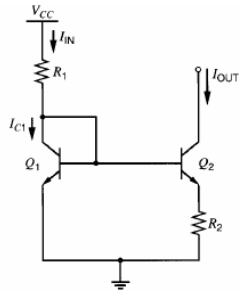
The Wilson current mirror is shown in Fig. 17, the cascode current mirror is shown in Fig. 18. Both circuits, the Wilson current mirror and the cascode current mirror achieve a very high output resistance. A small - signal analysis shows that R_o, with some approximations, has the value:

$$R_o \approx \frac{\beta_0 r_{o2}}{2}$$

In the cascode current mirror, the small-signal current that flows in the base of Q2 is mirrored through Q3 to Ql so that the small-signal base and emitter currents leaving Q2 are approximately equal.

On the other hand, in the Wilson current mirror, the small-signal current that flows in the emitter of Q2 is mirrored through Q1 to Q3 and then flows in the base of Q2. Although the cause and effect relationship here is opposite of that in a cascode current mirror, the output resistance is unchanged because the small-signal base and emitter currents leaving Q2 are still forced to be equal. Therefore, the small-signal collector current of Q2 that flows because of changes in the output voltage still splits into two equal parts with half flowing in $r_{\pi 2}$.

6. Bipolar Widlar Current Source - draw the schematic, explain why it is not a current mirror. pg. 300, course#8



(Abstract: In the Widlar current source the transistors Q_1 and Q_2 operate with unequal base emitter voltages. This circuit is referred to as a current source rather than a current mirror because the output current, I_{OUT}, is much smaller than the input current, I_{IN}.)

Fig. 19.

In the Widlar current source of Fig. 19, the resistor R_2 is inserted in series with the emitter of Q_2, and transistors Q_1 and Q_2 operate with unequal base emitter voltages if $R_2 \neq 0$. This circuit is referred to as a current source rather than a current mirror because the output current is much less dependent on the input current and the power-supply voltage than in the simple current mirror.

Assume that Q_1 and Q_2 operate in the forward active region. KVL around the base-emitter loop gives:

$$V_{BE1} - V_{BE2} - \frac{\beta_F + 1}{\beta_F} I_{OUT} R_2 = 0 \qquad \Rightarrow V_T \ln \frac{I_{C1}}{I_{S1}} - V_T \ln \frac{I_{OUT}}{I_{S2}} - \frac{\beta_F + 1}{\beta_F} I_{OUT} R_2 = 0$$

$$\text{If} \quad \beta \to \infty \quad \text{and} \quad I_{s1} = I_{s1} \qquad \Rightarrow V_T \ln \frac{I_{IN}}{I_{OUT}} = I_{OUT} R_2$$

This transcendental equation can be solved by trial and error to find I_{OUT} if R_2 and I_{IN} are known, as in typical analysis problems. Because the logarithm function compresses changes in its argument, attention can be focused on the linear term, I_{OUT} R_2, simplifying convergence of the trial-and-error process. In design problems, however, the desired I_{IN} and I_{OUT} are usually known, and the equations provides the required value of R_2.

The Widlar source allows currents in the microamp range to be realized with moderate values of resistance. It is possible to write the final equation like this:

$$I_{IN} = I_{OUT} e^{\frac{I_{OUT} R_2}{V_T}}$$

It is obvious that I_{OUT} is much smaller than I_{IN}.
Exemple: I_{IN} = 1 mA, R2= 5 KΩ, I_{OUT} = 20 μA

7. Temperature-Insensitive Bias with band gap voltage reference: the motive, the idea, one of the practical implementations. Pg. 317, course #9

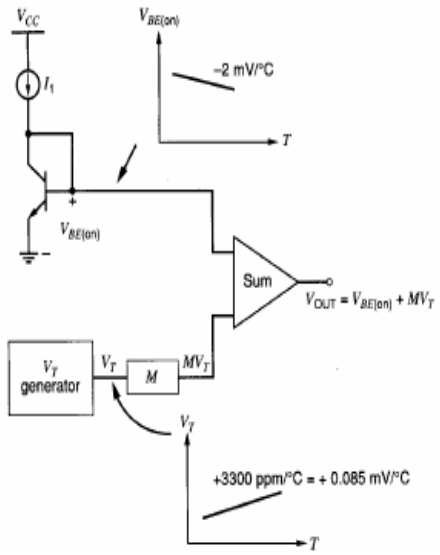


Fig. 20.

(Abstract: We need low-temperature-coefficient reference voltages. The idea is shown in Fig. 20. – 2mV/°C temperature-coefficient of V_{BE} to be compensated with a component with +2mV/°C coefficient temperature.)

In practice, requirements often arise for low-temperature-coefficient voltage bias or reference voltages. The voltage reference for a voltage regulator is a good example.

Since $V_{BE(on)}$ and V_T have opposite T_{CF}, the possibility exists for referencing the output current to a composite voltage that is a weighted sum of $V_{BE(on)}$ and V_T. By proper weighting, zero temperature coefficient should be attainable. So we can obtain low-temperature-coefficient voltage bias or reference voltages.

$$V_{OUT} = V_{BE(on)} + MV_T$$

The idea is shown in Fig. 20. – 2mV/°C temperature-coefficient of V_{BE} to be compensated with a component with +2mV/°C coefficient temperature. One possibility is to use V_T which T_{CF} is about +0,085 mV/°C.

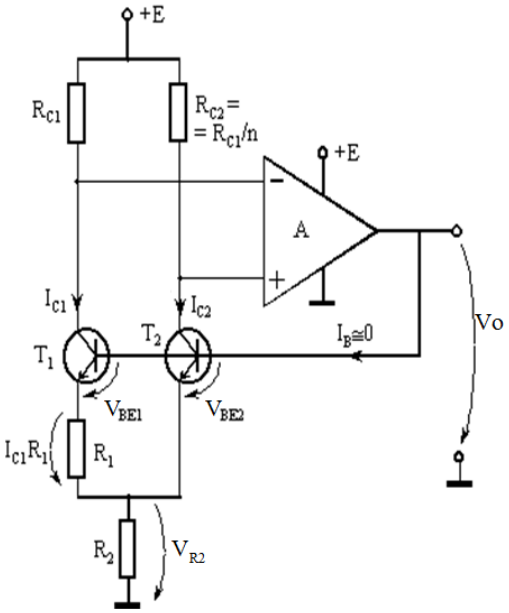


Fig. 21.

A bandgap voltage reference is a voltage reference circuit widely used in integrated circuits usually with an output voltage around 1.25 V, close to the theoretical band gap of silicon at 0°K. A practical implementation is shown in Fig. 21.

$$V_{RC1} = V_{RC2} \Rightarrow I_{C1} = I_{C2}$$

$$V_{R1} = I_{C1}R_1 = V_{BE2} - V_{BE1} =$$

$$= V_T \ln \frac{I_{C2}}{I_S} - V_T \ln \frac{I_{C1}}{I_S} = V_T \ln \frac{I_{C2}}{I_{C1}} = V_T \ln n$$

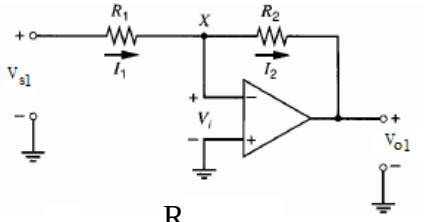
$$V_{R2} = R_2\left(I_{C1} + I_{C2}\right) = R_2\left(\frac{V_T \ln n}{R_1} + n\frac{V_T \ln n}{R_1}\right) =$$

$$= \frac{R_2}{R_1}(n+1)V_T \ln n = N \cdot V_T$$

$$\frac{dV_{R2}}{dT} = N\frac{dV_T}{dT} = N\frac{k}{q} = N\frac{kT}{qT} = N\frac{V_T}{T} = +2\frac{mV}{^\circ C} \qquad \Rightarrow N = 2\cdot 10^{-3}\frac{300}{26\cdot 10^{-3}} \cong 23$$

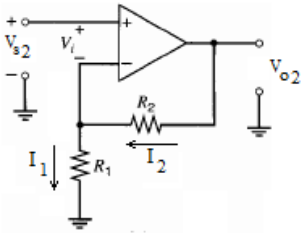
8. Inverting and noninverting amplifier built with an ideal op amp - draw the schematics and find the gains, define the characteristics of an ideal op amp. pg. 406, 408, course #9

(Abstract: The golden rules:
1.The output attempts to do whatever is necessary to make the voltage difference between the inputs zero (in Fig. 22 and Fig. 23, $V_i = 0$).
2.The inputs draw no current.)



$$V_{o1} = -V_{s1}\frac{R_2}{R_1}$$

Fig. 22.



$$V_{o2} = \left(1 + \frac{R_2}{R_1}\right)V_{s2}$$

Fig. 23.

An ideal op amp with a single-ended output has a differential input, infinite voltage open-loop gain, infinite input resistance, and zero output resistance. While actual op amps do not have these ideal characteristics, their performance is usually sufficiently good that the circuit behavior closely approximates that of an ideal op amp in most applications. These characteristics lead to the golden rules for op-amps. They allow us to logically deduce the operation of any op-amp circuit.

Fig. 22 shows an inverting amplifier build with an op amp. Considering we have an ideal op amp. First, because no current enters in the "-" input, at the nod X we can write:

$$I_1 = I_2 \qquad (1)$$

Second, $V_i = 0$ and at the inverting input we have a " virtual ground". Then the voltage V_{s1} is across R_1 and Vo1 is across R_2. In the first equation we can replace I_1 and I_2 with the values:

$$I_1 = \frac{V_{s1}}{R_1} \qquad I_2 = \frac{-V_{o1}}{R_2}$$

Equation (1) becames:

$$\frac{V_{s1}}{R_1} = -\frac{V_{o1}}{R_2} \Leftrightarrow V_{o1} = -V_{s1}\frac{R_2}{R_1}$$

This is the relationship between the output voltage and the input voltage for an inverting amplifier build with an op amp. A similar calculation can be done for the noninverting amplifier build with an ideal op amp (Fig. 23). The same, for Fig. 23:

$$I_1 = I_2 \qquad (2)$$

But we don't have a virtual ground anymore: at the noninverting input is V_{s2}. In this case we can write:

$$I_1 = \frac{V_{s2}}{R_1} \qquad I_2 = \frac{V_{o2} - V_{s2}}{R_2}$$

Using this values in (2) we get the relationship between the output voltage and the input voltage for a noninverting amplifier build with an op amp:

$$\frac{V_{s2}}{R_1} = \frac{V_{o2} - V_{s2}}{R_2} \Leftrightarrow V_{o2} = \left(1 + \frac{R_2}{R_1}\right)V_{s2}$$

9. Integrator, differentiator build with op amp - draw the schematics, find the relationships between input and output voltages. pg. 410, Course #10

The integrator (Fig. 24) and the differentiator circuits (shown in Fig. 25) are examples of using op amps with reactive elements in the feedback network to realize a desired frequency response or time-domain response.

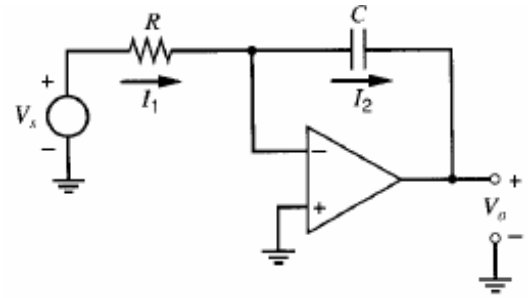


Fig. 24.

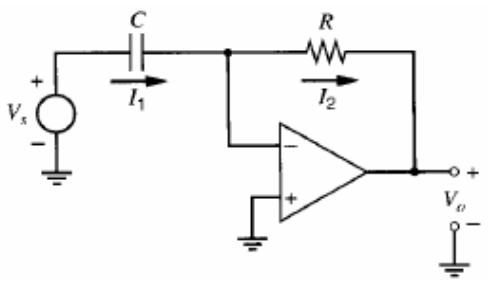


Fig. 25.

(Abstract: In the case of the integrator the output voltage is proportional to the integral of the input voltage with respect to time. In the case of the differentiator the output voltage is proportional to the time rate of change of the input voltage.)

In the case of the integrator (Fig. 24), the resistor R is used to develop a current I_1 that is proportional to the input voltage, V_s. This current flows into the capacitor C, whose voltage is proportional to the integral of the current I_2 with respect to time. Since the output voltage is equal to the negative of the capacitor voltage, the output is proportional to the integral of the input voltage with respect to time. In terms of equations:

$$I_1 = \frac{V_s}{R} = I_2 \qquad V_o = -\frac{1}{C}\int_0^t I_2 d\tau + V_o(0) \quad \Rightarrow V_o(t) = -\frac{1}{RC}\int_0^t V_s(\tau)d\tau + V_o(0)$$

In the case of the differentiator (Fig. 25), the capacitor C is connected between V_s and the inverting op-amp input. The current through the capacitor is proportional to the time derivative of the voltage across it (V_c), which is equal to the input voltage ($V_c = V_s$). This current flows through the feedback resistor R, producing a voltage at the output proportional to the capacitor current, which is proportional to the time rate of change of the input voltage. In terms of equations:

$$I_1 = C\frac{dV_s}{dt} = I_2 \qquad V_o = -RI_2 = -RC\frac{dV_s}{dt}$$

10. Improved precision half-wave rectifier - draw the schematic, the equivalent ones, the diadrames and explain the operation. pg.705, Course #10

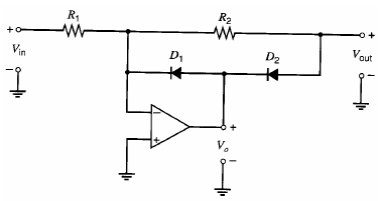


Fig. 26.

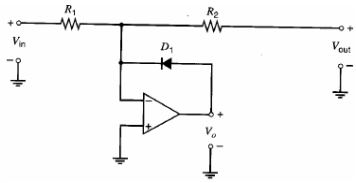


Fig. 27.

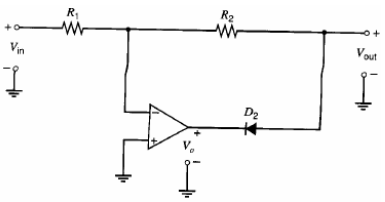


Fig. 28.

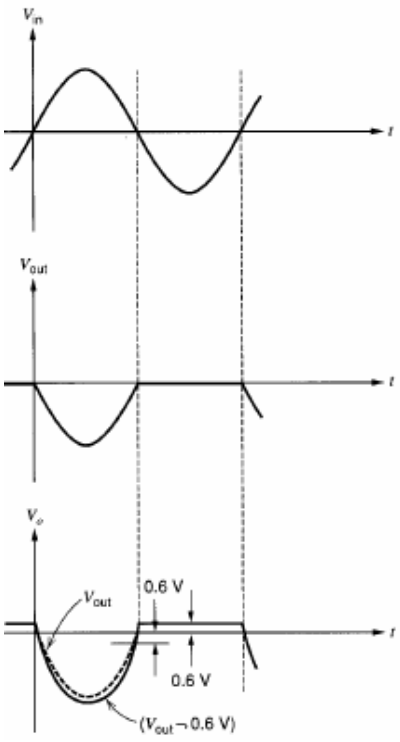


Fig. 29.

(Abstract: The schematic for an improved precision half-wave rectifier is shown in Fig. 26. Fig. 27 shows the equivalent circuit for $V_i<0$ and Fig. 28 shows the equivalent circuit for $V_i>0$. Fig. 29 shows the waveforms within the improved precision rectifier for a sinusoidal input, V_{in}; the output of the circuit is V_{out} and V_o is the op amp's output.)

For input voltages less than zero, the equivalent circuit is shown in Fig. 27. Diode D_1 is forward biased and the op amp is in the active region. The inverting input of the op amp is clamped at ground by the feedback through D_1, and, since no current flows in R_2, the output voltage is also at ground.

When the input voltage is made positive, no current can flow in the reverse direction through D_1 so the output voltage of the op amp V_o is driven in the negative direction. This reverse biases D_1 and forward biases D_2. The resulting equivalent circuit is shown in Fig. 28 and is simply an inverting amplifier with a forward-biased diode in series with the output lead of the op amp.

Because of the large gain of the op amp, this diode has no effect on its behavior as long as it is forward biased, and so the circuit behaves as an inverting amplifier giving an output voltage of:

$$V_{out} = -\frac{R_2}{R_1} V_{in}$$

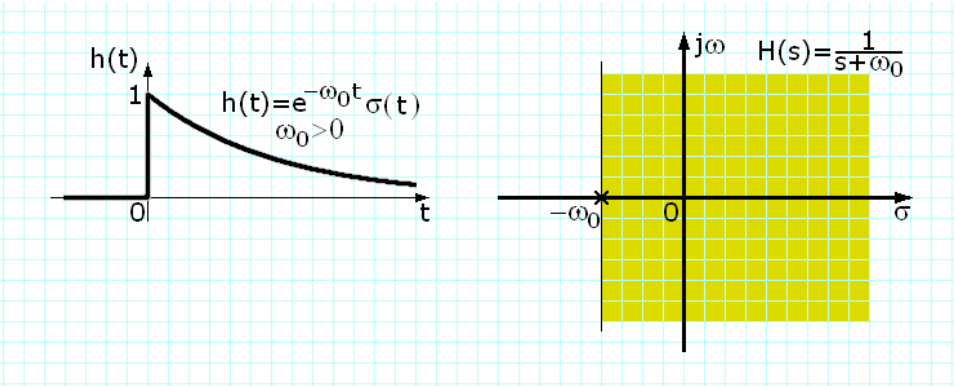
As shown in Fig. 29, the output voltage of the operational amplifier need only change in value by approximately two diode drops when the input signal changes from positive to negative.

1. **Where are the poles of a stable and causal analog system? Give an example.**

The poles of a stable and causal system are located in the left half plane LHP while its zeros can be located anywhere in the complex plane. Example: $h(t)=\exp(-\omega_0 t)\sigma(t),\omega_0>0$.

[1] -page 110

The transfer function is $H(\omega)=\frac{1}{s+\omega_0}$ with one pole, $s_p=-\omega_0$.



2. **Define minimum phase analog systems. Give an example.**

[1] -page 127

Systems having poles and zeros placed in the left half plane are named minimum phase systems. Consider the system with the impulse response

$h(t)=e^{-t}\sigma(t)\leftrightarrow H_u(s)=\frac{1}{s+1}$. It has one pole in the LHP and no zeros; hence it is a minimum phase system:

$H(\omega)=\frac{1}{1+j\omega}$, with $|H(\omega)|=1/\sqrt{1+\omega^2},\Phi(\omega)=-arctg\omega$.

as opposed to another system with the frequency response:

$$H_{\omega_0}(\omega)=\frac{1}{1+j\omega}\frac{1-j\frac{\omega}{\omega_0}}{1+j\frac{\omega}{\omega_0}}\longleftrightarrow h_{\omega_0}(t)=\frac{1}{\omega_0-1}\left[(\omega_0+1)e^{-t}-2\omega_0 e^{-\omega_0 t}\right]\sigma(t)$$

with $\Phi_{\omega_0}(\omega)=-arctg\omega-2arctg\frac{\omega}{\omega_0}=\Phi(\omega)-2arctg\frac{\omega}{\omega_0}$.

Both systems have the same amplitude-frequency characteristic but the second system introduces extra phase versus the first system.

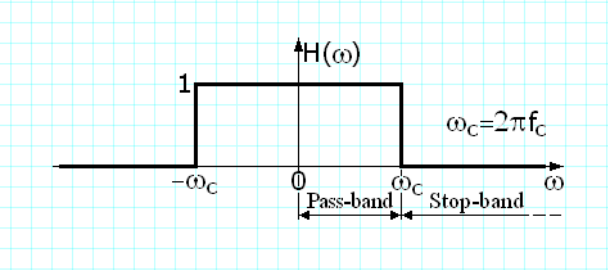
3. **Ideal low pass filter. Frequency response and impulse response. Is this filter realizable?**

[1]-page 134

The ideal low pass filter has the frequency response:

$$H(\omega)=p_{\omega_c}(\omega)\leftrightarrow h(t)=\frac{\sin\omega_c t}{\pi t}$$

It does not fulfill Paley-Wiener theorem, so it is not causal.



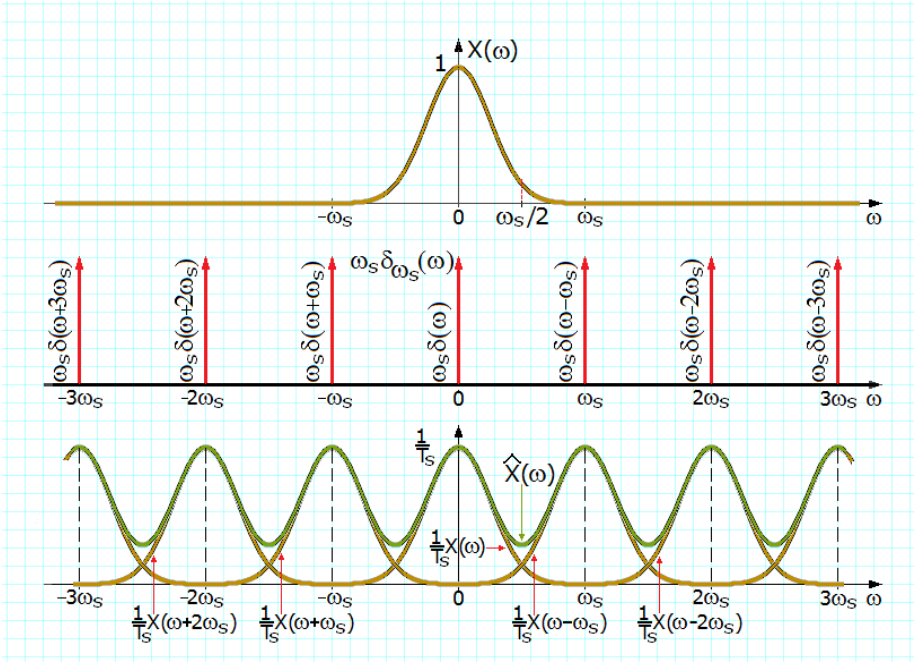
4. Enunciate WKS sampling theorem.

[1]-page 150

If the finite energy signal $x(t)$ is band limited at ω_M , ($X(\omega)=0$ for $|\omega| > \omega_M$), it is uniquely determined by its samples $\{x(nT_s)|n \in \square\}$ if the sampling frequency is higher or equal than twice the maximum frequency of the signal:

$$\omega_s \geq 2\omega_M$$

5. Spectrum of ideal sampled signal (Relation + Graphical representation).



Spectrum of original signal

Spectrum of periodic Dirac distribution

Spectrum of ideal sampled signal

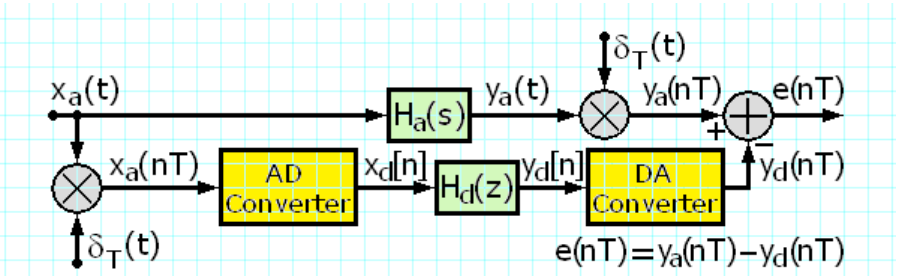
[1]-page 146

$$x(t)=\sum_{k=-\infty}^{\infty} x(kT_s)\delta(t-kT_s) \leftrightarrow \hat{X}(\omega)=\frac{1}{T_S}\sum_{k=-\infty}^{\infty} X\left(\omega-k\frac{2\pi}{T_S}\right)$$

The spectrum of an ideal sampled signal is the periodic repetition of the spectrum of the original signal. The period is inverse proportional with the sampling step T_S.

6. Approximation of continuous-time systems with discrete-time systems using impulse invariance method.

[1]-page 236, page 244



The system (not necessarily band-limited) is identified using input signal of the analog system the Dirac impulse. The impulse response of the analog system is sampled to produce the impulse response of the digital system.

for $x_a(t)=\delta(t)\Rightarrow y_a(t)=h_a(t)$; $x_d[n]=\frac{1}{T}\delta[n]$; $y_a(nT)=h_a(nT)$.

$$y_d[n]=\frac{1}{T}\delta[n]*h_d[n]=\frac{1}{T}h_d[n]$$

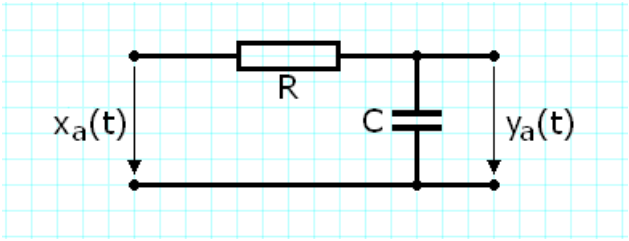
The error is smallest for: $h_d[n]=Th_a(nT)$

The frequency response of the digital system is the same with the frequency response of the analog system of limited band for frequency less than half of the sampling frequency

$$H_a(\omega)=H_d(\Omega)\big|_{\Omega=\omega T};\quad |\omega|\le\frac{\pi}{T}\quad\text{and}\quad \omega_M\le\frac{\pi}{T}$$

7. Approximation of RC circuit using bilinear transform method.

[1]-page 265



time constant: $\tau=RC=\frac{1}{\omega_0}$; $H_a(s)=\frac{1}{1+s\tau}$

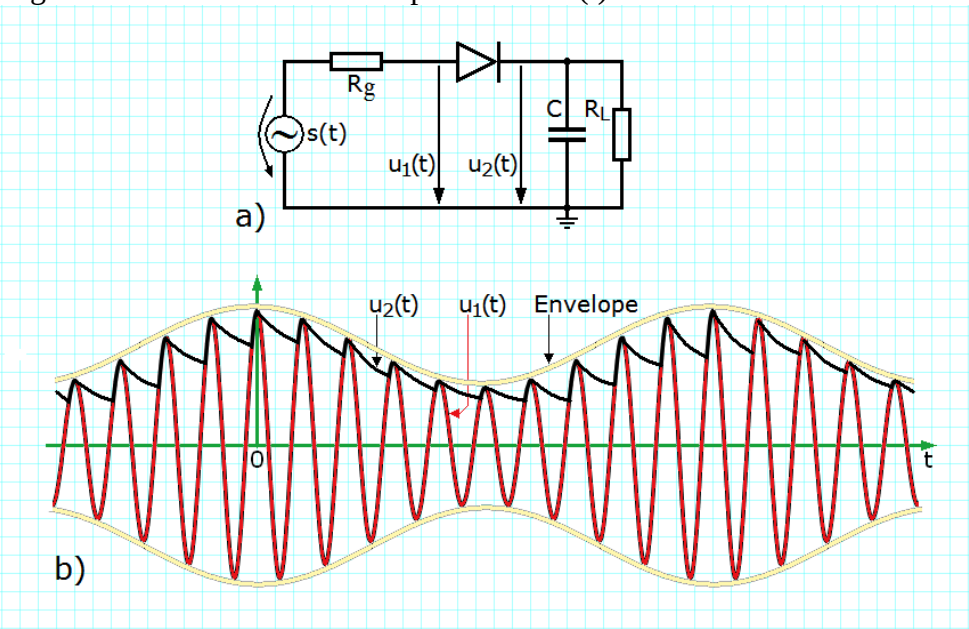
$$s=\frac{2}{T}\frac{1-z^{-1}}{1+z^{-1}};\qquad H_d(z)=H_a(s)\Big|_{s=\frac{2}{T}\frac{1-z^{-1}}{1+z^{-1}}}$$

$$\Rightarrow H_d(z)=\frac{\frac{T}{T+\tau}}{1-\frac{\tau}{T+\tau}z^{-1}}$$

8. Demodulator (envelope detector) for AM signals.

[1]-page 275

AM demodulation can be realized using an envelope detector. For $R_g << R_s$, the voltage from the capacitor $u_2(t)$ follows the voltage $u_1(t)$ if the latter is high enough and the diode conducts (on the positive half-cycle of the input signal). When the diode becomes reverse biased, the capacitor discharges through the resistor R_L. The modulating wave is reconstructed using low pass filtering and removal of the DC component for $u_2(t)$.



9. Narrow Band Frequency Modulation.

[1]-page 298

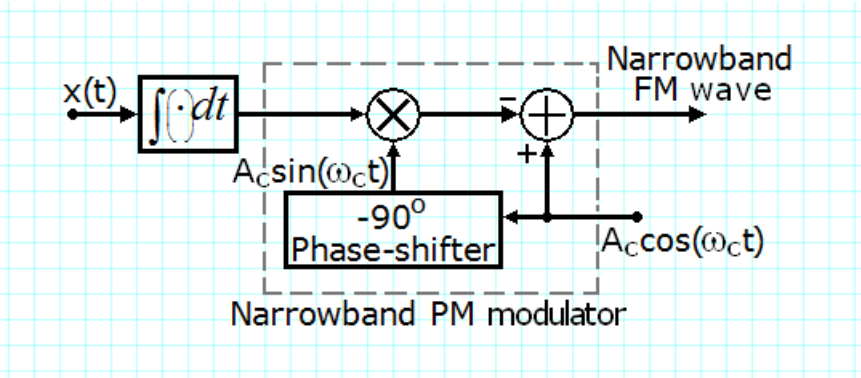
FM signal's expression is: $s(t) = A_c \cos\theta_i(t) = A_c \cos\left[\omega_c t + \beta \sin \omega_m t\right]$, where the modulating wave to be transmitted is $x(t) = A_m \cos \omega_m t$. Depending on the value of the modulation index $\beta = \Delta\omega / \omega_m$, we have narrow band FM ($\beta << 1$ radian) or wide band FM ($\beta >> 1$ radian). For narrow band FM, the modulated wave is:

$s(t) = A_c \cos\omega_c t \cos(\beta \sin \omega_m t) - A_c \sin\omega_c t \sin(\beta \sin \omega_m t).$

If $\beta < \dfrac{\pi}{36}$ rad $\Rightarrow \cos(\beta \sin \omega_m t) \cong 1$ and $\sin(\beta \sin \omega_m t) \cong \beta \sin \omega_m t$

$\Rightarrow s(t) = A_c \cos\omega_c t - \beta A_c \sin\omega_c t \sin\omega_m t.$

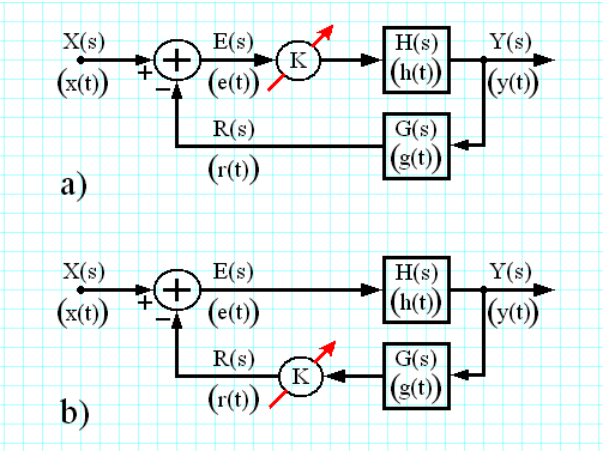
A possible implementation scheme is shown below.



There are two disadvantages:
1-the envelope is affected by residual amplitude modulation so it varies in time,
2-for a harmonic modulating wave, the angle $\theta_i(t)$ contains other harmonics (order 3 and superior) of the modulating frequency, ω_m, so it is distorted.

10. Nyquist stability criterion for continuous-time systems when the open loop system is stable (schema + enunciation).

[1]-page 350, page 372

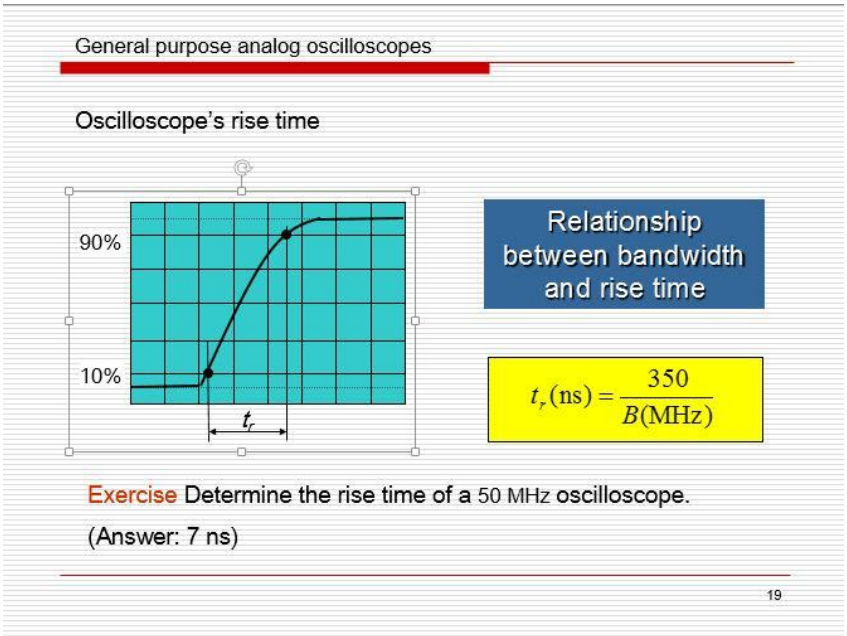


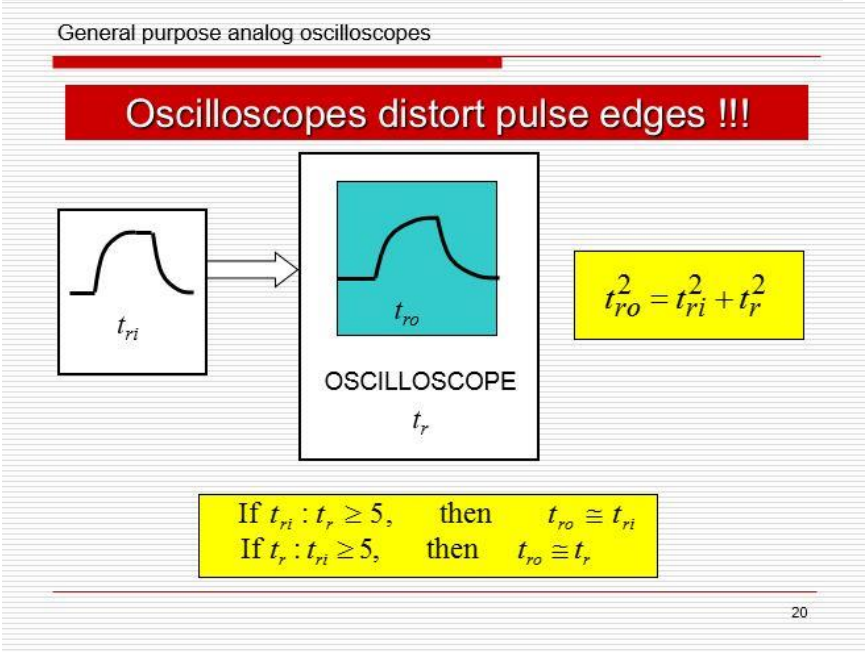
a) $\frac{Y(s)}{X(s)} = \frac{KH(s)}{1+KH(s)G(s)}$

b) $\frac{Y(s)}{X(s)} = \frac{H(s)}{1+KH(s)G(s)}$

-If the open loop system is stable then $H(s)G(s)$ doesn't have poles in the right half plane or on the imaginary axis. So, the open loop Nyquist's hodograph $G(j\omega)H(j\omega)$ **doesn't make complete rotations** around the point (-1/K,0)
-Since $h(t)$ and $g(t)$ are real functions, Nyquist's hodograph for $\omega \in (-\infty,0)$ is obtained by **symmetry** with respect to the real axis of the complex plane $H(s)G(s)$ from the Nyquist's hodograph for $\omega \in (0,\infty)$

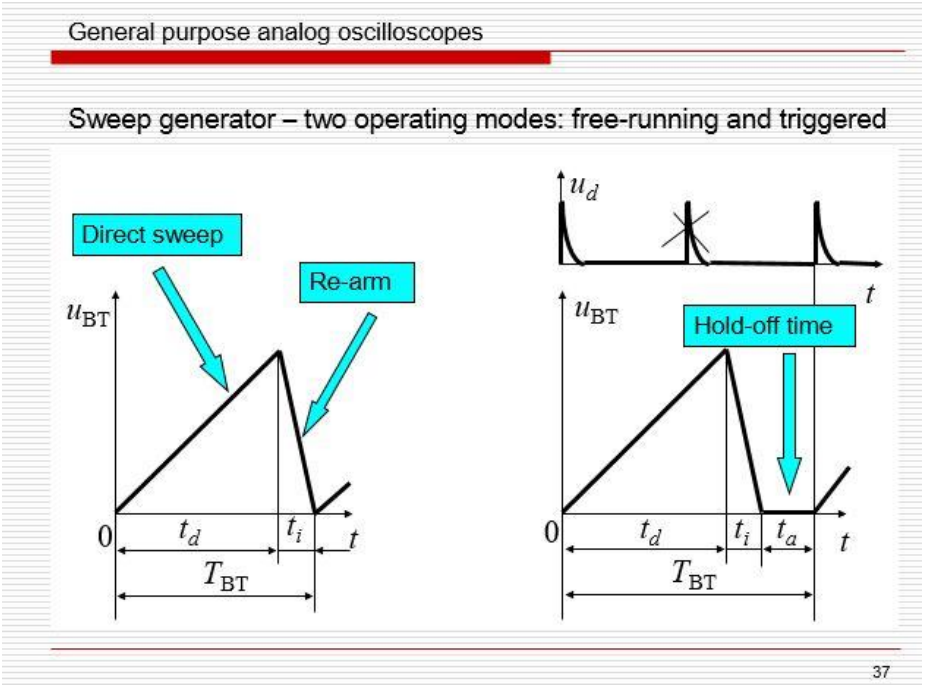
1. **General purpose analog oscilloscopes.** Relationship between bandwidth and rise time of an oscilloscope. Relationship between rise time of an oscilloscope and rise time of a pulse.



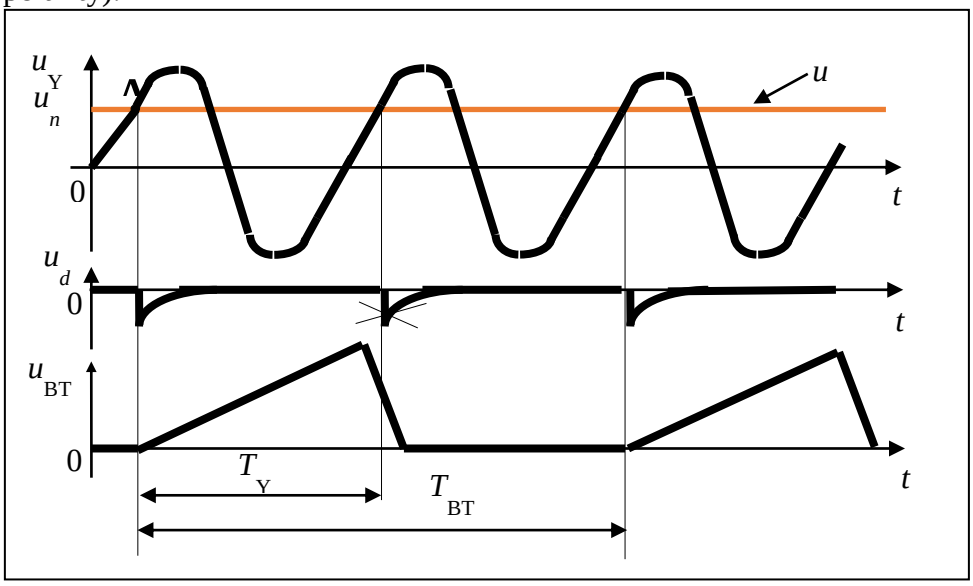


https://intranet.etc.upt.ro/~E_INSTR/Documentation_2015-2016/, Ch1_ Oscilloscopes_c1-c3_2015.ppt - slide #19-20

2. **General purpose analog oscilloscopes.** Describe the free-running and the triggered modes of operation of the time base.



With triggered sweeps, the scope will blank the beam and start to reset the sweep circuit (re-arm) each time the beam reaches the extreme right side of the screen.
For a period of time, called *hold-off*, the sweep circuit resets completely and ignores triggers. Once hold-off expires, the next trigger starts a sweep.
The trigger event is usually the input waveform reaching some user-specified threshold voltage (trigger level) in the specified direction (going positive or going negative - trigger polarity).



Triggering circuit - ensures a stable image on the screen
Triggering condition - The sweep generator's period should be a multiple of the signal period: $T_{BT} = kT_Y$

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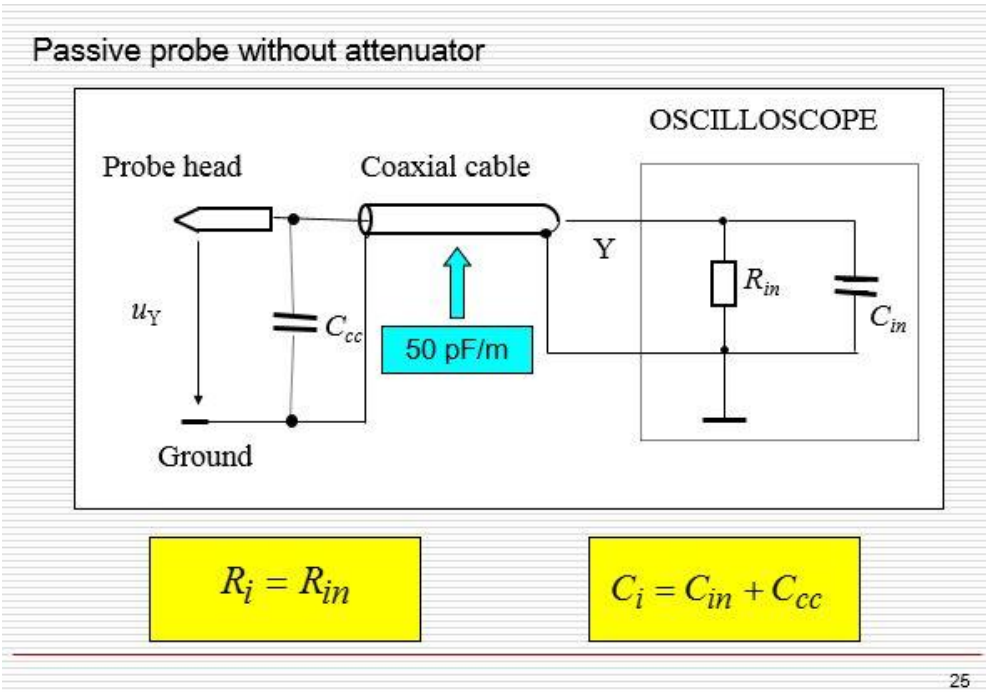
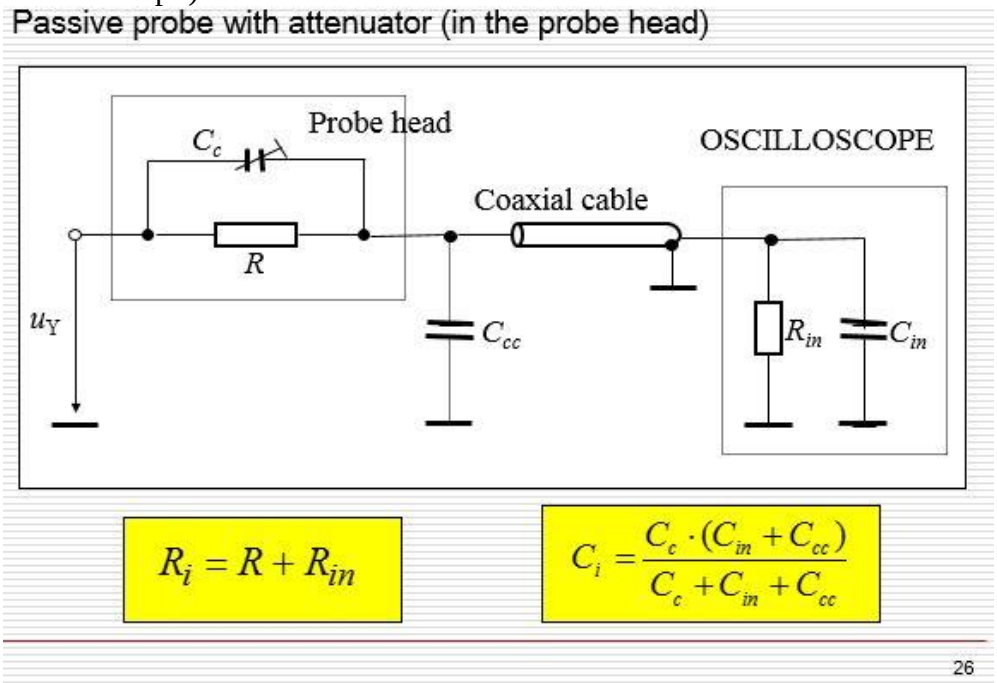
3. Probes for oscilloscopes without and with attenuator – comparison



Advantage – it does not attenuate the input signal
Disadvantage – relatively small input resistance (1 MΩ), large input capacitance (50 - 150 pF)



Advantage – large input resistance (10 MΩ), small input capacitance (5 - 15 pF)
Disadvantage – it attenuates the input signal (therefore, the value read on the display must be multiplied by the probe's attenuation factor)

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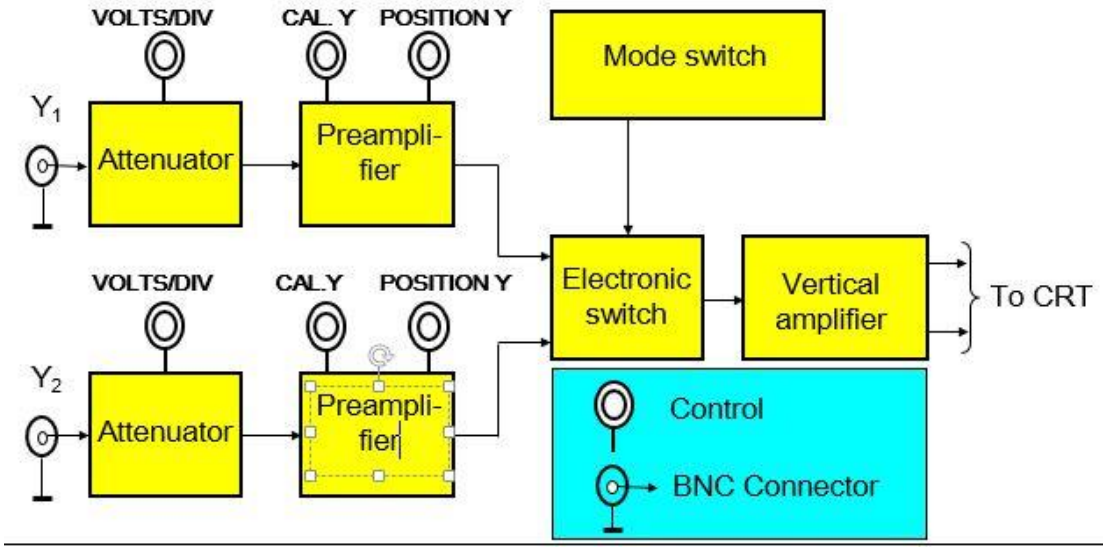
4. **Dual-trace oscilloscopes - the electronic switch** –block diagram, operating modes



Dual-trace oscilloscopes have a **mode switch** to select either channel alone, both channels, or (in some oscilloscopes) an X-Y display, which uses the second channel for X deflection.

When both channels are displayed, the type of **channel switching** can be selected on some oscilloscopes; on others, the type depends upon timebase setting. If manually selectable, channel switching can be free-running (asynchronous), or between consecutive sweeps.

Operating modes

- Y_1 – input to channel one is displayed
- Y_2 – input to channel two is displayed
- CHOPPED – signals on both channels are displayed.
  Channel switching is free-running (asynchronous), with a fixed frequency of some hundreds of kHz. Recommended for low frequency signals.
- ALTERNATE – signals on both channels are displayed.
  Channel switching is done between consecutive sweeps.
  Recommended for high frequency signals.

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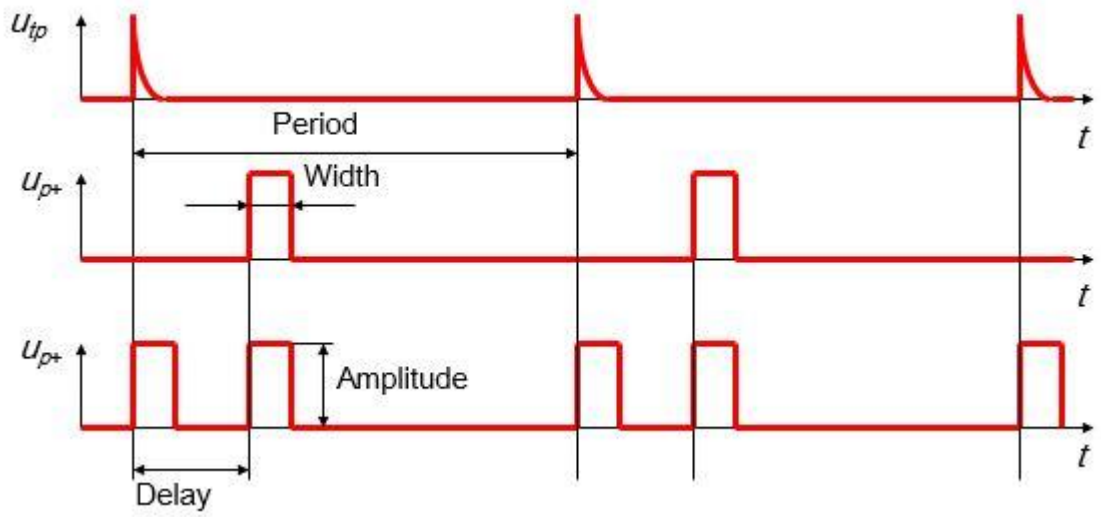
5. **Signal generators.** Describe the operation of the pulse generator in normal, internally triggered, single and double pulses modes.

Operating modes: Normal, internally triggered, simple positive pulses

The trigger block operates autonomously and sets the repetition rate of the generated pulses.

The generator provides, in each cycle, a trigger pulse and one pulse at each output (positive and negative), delayed with respect to the trigger pulse.



In double pulses mode the generator provides, in each cycle, a trigger pulse and two pulses at each output. The first pulse is generated at the same time with the trigger pulse, and the second one is delayed with respect to the trigger pulse.

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6. **Signal generators.** Principle of a Direct Digital Synthesis generator – advantages and disadvantages.

DDS (direct digital synthesis) is a technique used in function/arbitrary waveform generators to produce an analog waveform, such as a sine wave. Involve generating a time-varying signal represented in a digital format and then performing a digital-to-analog conversion to convert the digital data into an analog output.

The main performance advantages of using DDS technology are:

- Waveform frequency changes are phase-continuous
- Waveform frequency changes are very fast without unwanted effects
- Frequency resolution is digitally controlled and very good (μHz)
- Frequency modulation, phase modulation, and frequencysweeps are easily implemented
- Many of the problems associated with analog architectures are eliminated due to the digital nature of DDS

A few significant disadvantages:

- The number of points in a waveform must be equal to an exact power of two
- Increased waveform jitter and distortion are possible

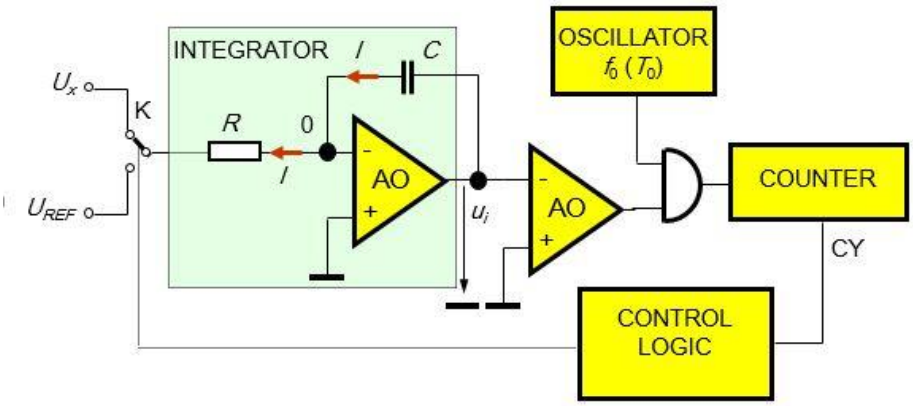
https://intranet.etc.upt.ro/~E_INSTR/Documentation_2015-2016/, Ch2_Signal Generators_c7-8_2015.ppt- slide #38-41

7. **Digital voltmeters and multimeters.** Specify the measurement result for a 100% confidence level (result ± uncertainty, confidence level) according to the rules for data presentation when measuring a voltage of 12.45 V with a 3 ½ digit 20 V voltmeter whose maximum permissible error is given by Δ_t=0,1% × reading + 0,05% × range + 1 digit.

The DVM reads xx.xx V. Therefore,

1 digit = 10 mV.
The maximum permissible error when measuring 12.45 V is
Δ_t=0,1% × 12.45 V + 0,05% × 20 V + 10 mV,
or
Δ_t=12.45 mV + 10 mV + 10 mV = 32.45 mV.
For a confidence level of 100%, the measurement result should be specified as
U = 12.45 V ± 0.03 V
https://intranet.etc.upt.ro/~E_INSTR/Documentation_2015-2016/, Ch3_Digital Voltmeters and Multimeters_c9-10_2015.ppt - slide #8-10

8. **Digital voltmeters and multimeters.** Dual slope ADC – block diagram, operation principle, relationships

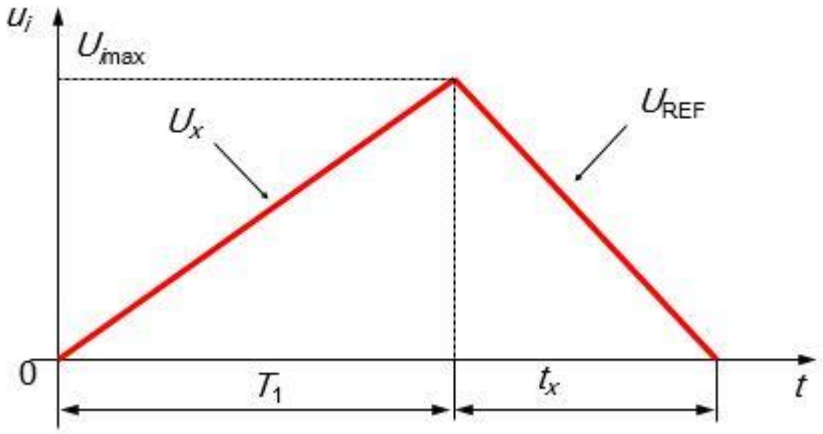


Operation of the converter comprises two steps (phases): (1) integration of the unknown input voltage and (2) integration of a known reference voltage, of opposite polarity. Phase 1 has a fixed duration, denoted T1. At the end of this phase, the integrator's output voltage is the same as the voltage across the capacitor. The second phase starts at t = T1. Switch K now feeds the reference voltage UREF at the integrator's input. This leads to the so called de-integration and it ends when the integrator's output nulls.

$$U_{i\max} = \frac{U_x}{RC} T_1 \qquad T_1 = N \cdot T_0$$

$$U_{i\max} = \frac{U_{REF}}{RC} t_x \qquad t_x = n \cdot T_0$$

$$U_x \cdot T_1 = U_{REF} \cdot t_x \qquad U_x = \frac{n}{N} U_{REF}$$



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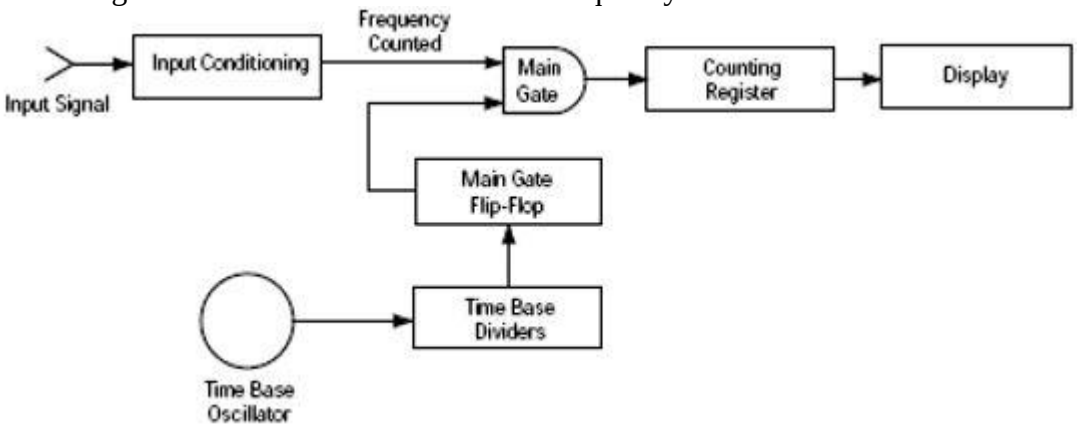
https://intranet.etc.upt.ro/~EEM/PDFuri/Electrical%20and%20Electronic%20Measurements%20Chapter%202.pdf pages #70-73.

9. **Universal counters.** Describe the operating principle and explain how frequency can be measured.

The frequency f of a repetitive signal can be defined by the number of cycles of that signal per unit of time: f=n/t, where n is the number of cycles and t is the time interval in which they occur. As suggested by the above equation, the frequency can be measured by counting the number of cycles and dividing it by t.
By taking t equal to one second, the number of counted cycles will represent the frequency (in Hz) of the signal.

Block diagram of a universal counter in the frequency measurement mode:



The input signal is initially conditioned to a form that is compatible with the internal circuitry of the counter. The conditioned signal is a pulse train where each pulse corresponds to a cycle of the input signal. With the main gate open, pulses are allowed to pass through and get totalized by the counting register.

The time base oscillator together with the decade dividers and the main gate flip flop control the opening time of the main gate.

As mentioned before, if T2=1s, the counting register will read the frequency of the input signal (measurement resolution of 1 Hz).

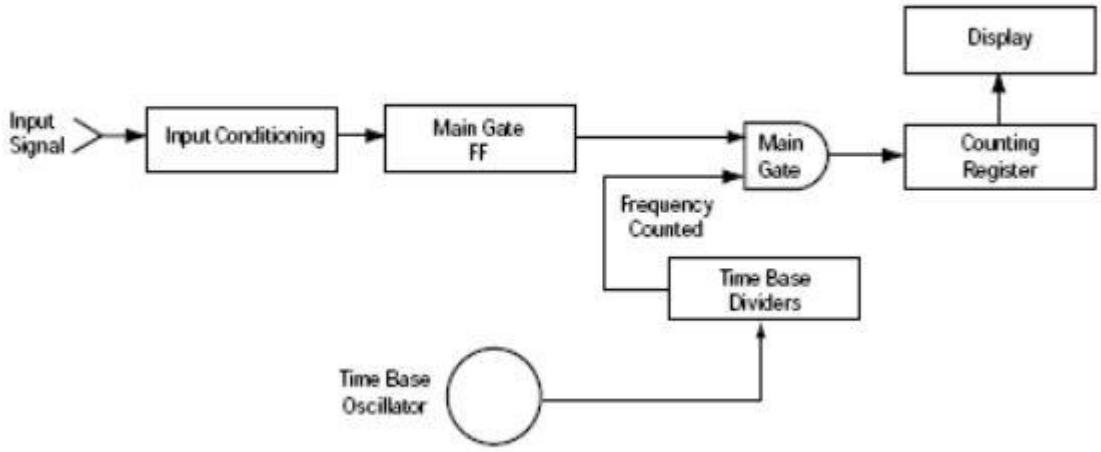
https://intranet.etc.upt.ro/~E_INSTR/Documentation_2015-2016/, Ch4_Universal counters_2015.ppt, slides #8-11

10. **Universal counters.** Describe the operating principle and explain how period can be measured.

The period of a signal is the time taken by the signal to complete a cycle of oscillation.

The input signal is initially conditioned to a form that is compatible with the internal circuitry of the counter. The conditioned signal is a pulse train where each pulse corresponds to a cycle of the input signal. In the period measurement mode, the main gate is open for one period of the input signal and the counting register totalizes the pulses provided by the time base. If the period of the pulses provided by the time base is 1 μs, the number totalized by the counting register will represent the period of the input signal in microseconds.

Basic block diagram of a universal counter in the period measurement mode



Used for more accurate measurement of unknow low-frequency signals - increased resolution.

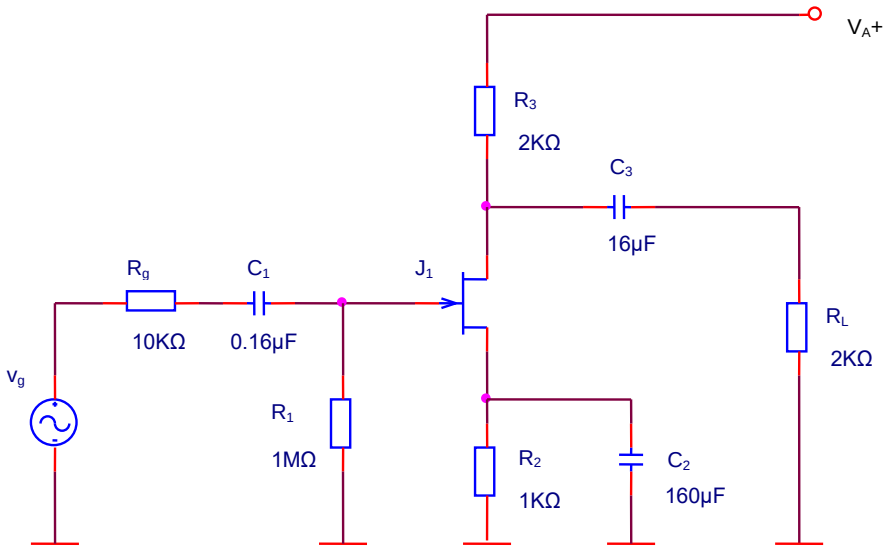
https://intranet.etc.upt.ro/~E_INSTR/Documentation_2015-2016/, Ch4_Universal counters_2015.ppt, slides #12-13

5TH THEMATIC AREA – S11, S12

CASE STUDIES / PROBLEMS / PROJECTS

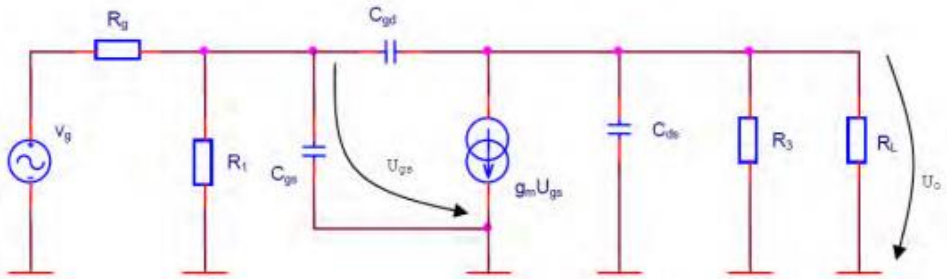
ELECTRONIC CIRCUITS

1. (15p) For the circuit below, having the J-FET with parameters: g_m = 5mA/V, $r_{ds} = \infty$, C_{gd} = 5pF, C_{gs} = 10pF, C_{ds} = 10pF.
Find out the high cutt off frequency by:
a) Using Miller Theorem;
b) Using OCTC (Open Circuit Time Constant) method.

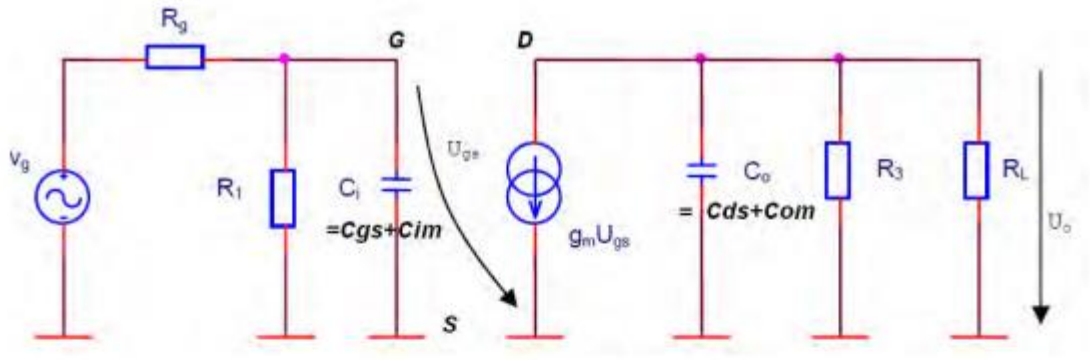


Solution:

a) First must draw equivalent schematic for small signal, mean frequencies:



By using Miller theorem, Cgd cand be splitted in 2 capacitors to ground Cim and Com, which will add to existing Cgs respective Cds, resulting in Ci and Co as below:



Gain K between G and D is needed to estimate Cim and Com capacitances:

$$K = \frac{U_o}{U_i} \text{ şi } U_o = -g_m U_{gs}(R_3 \| R_L),\ U_i = U_{gs} \Rightarrow K = A_{U0} = -g_{ms} R_3 \| R_L = -5$$

Then according to Miller:

$$C_{iM} = C_{gd}(1-K) = 30 \text{ pF},\ C_{oM} = C_{gd}\left(1 - \frac{1}{K}\right) = 6 \text{ pF}$$

$$C_i = C_{gs} \| C_{iM} = C_{gs} + C_{iM} = 40 \text{ pF},\ C_o = C_{ds} \| C_{oM} = C_{ds} + C_{oM} = 16 \text{ pF}$$

Cutt of (pole) frequencies introdeced by these capacitors are:

$$f_{P1} = \frac{1}{2 \cdot \pi \cdot C_i \cdot R_{P1}},\ R_{P1} = R_g \| R_1 \cong R_g \cong 10K\Omega \Rightarrow f_{P1} = 400KHz$$

$$f_{P2} = \frac{1}{2 \cdot \pi \cdot C_o \cdot R_{P2}},\ R_{P2} = R_3 \| R_L = 1K\Omega \Rightarrow f_{P2} = 10MHz\ .$$

Transfer function by neglecting zero frequency introduced by Cgs will be:

$$A_U(j\omega) = -5 \cdot \frac{1}{(1 + j\frac{f}{0.4 \cdot 10^6}) \cdot (1 + j\frac{f}{10 \cdot 10^6})}$$

Transfer function by neglecting zero frequency introduced by Cgs will be:

$$A_U(j\omega) = -5 \cdot \frac{1}{(1 + j\frac{f}{0.4 \cdot 10^6}) \cdot (1 + j\frac{f}{10 \cdot 10^6})}$$

High cutt of frequency will have aproximative value:

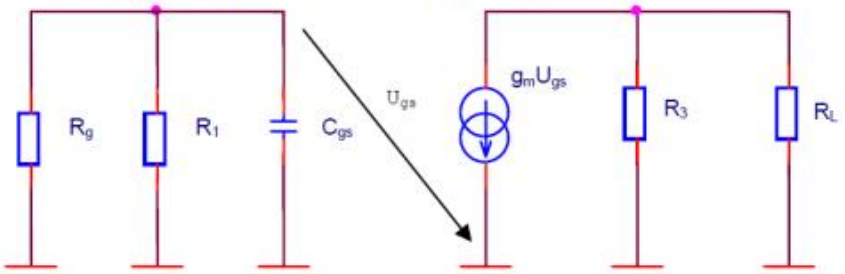
$$f_{P1} = 400\text{KHz}$$

Or can be computed exactly considering the 3db attenuation at cutt of frequency:

$$\left|A_U(j\omega)\right\|_{f=f_i} = \frac{1}{\sqrt{2}} A_{U0} \Rightarrow f_i = 393{,}7\text{KHz}$$

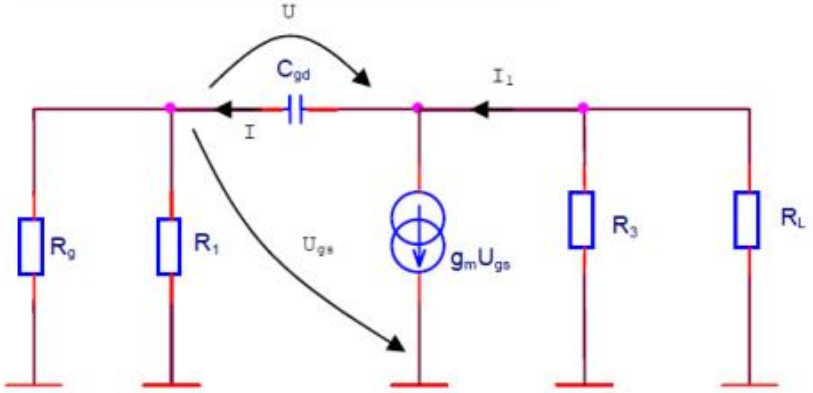
b) If OCTC is applied to first schematic (without to get benefit of Miller theoreme), involve to evaluate 3 time constants, one for each capacitor as folows:

- **Cgs effect**, all the others C = open circuit:



$$f_{P1} = \frac{1}{2 \cdot \pi \cdot C_{gs} \cdot R_{P1}}, R_{P1} = R_1 \| R_g \cong R_g \cong 10K \Rightarrow f_{P1} = 1{,}6MHz$$

- **Cgd effect**, all the others C = open circuit:



$$f_{P2} = \frac{1}{2 \cdot \pi \cdot C_{gd} \cdot R_{P2}}$$

Equivalent resistance between Cgd nodes can be found if Cgd is replaced with a voltage source U:

$$R_{P2} = \left| \frac{U}{I} \right|$$

Using Kirchhoff laws :

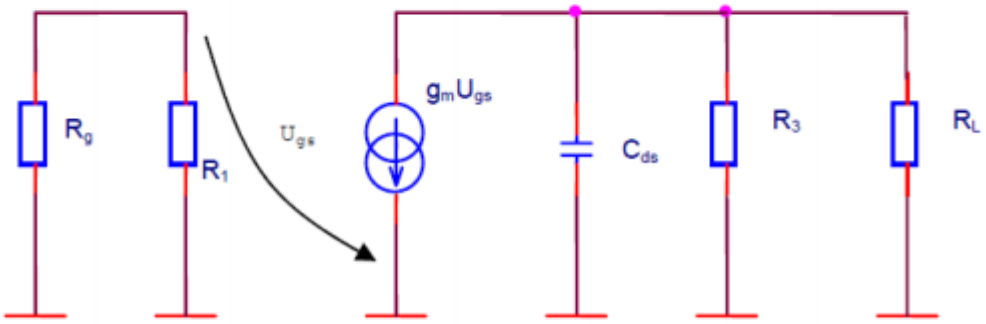
$$-i \cdot R_g \| R_1 + u_{gs} = 0 \Rightarrow u_{gs} = i \cdot R_g \| R_1$$

$$I_1 = g_m \cdot u_{gs} + I = I(1 + g_m \cdot R_g \| R_1)$$

$$U - I \cdot R_g \| R_1 - I_1 \cdot R_3 \| R_L = 0 \Rightarrow U = I \cdot R_g \| R_1 + I \cdot (1 + g_m \cdot R_g \| R_1) \cdot R_3 \| R_L$$

$$R_{P2} = \frac{U}{I} = R_g \| R_1 + (1 + g_m \cdot R_g \| R_1) \cdot R_3 \| R_L = 61\text{K}\Omega. \Rightarrow f_{P2} = 524{,}6KHz$$

➢ **Cds effect**, all the others C = open circuit:



$$f_{P3} = \frac{1}{2 \cdot \pi \cdot C_{ds} \cdot R_{P3}},\ R_{P3} = R_3 \| R_L = 1K \Rightarrow f_{P3} = 16MHz$$

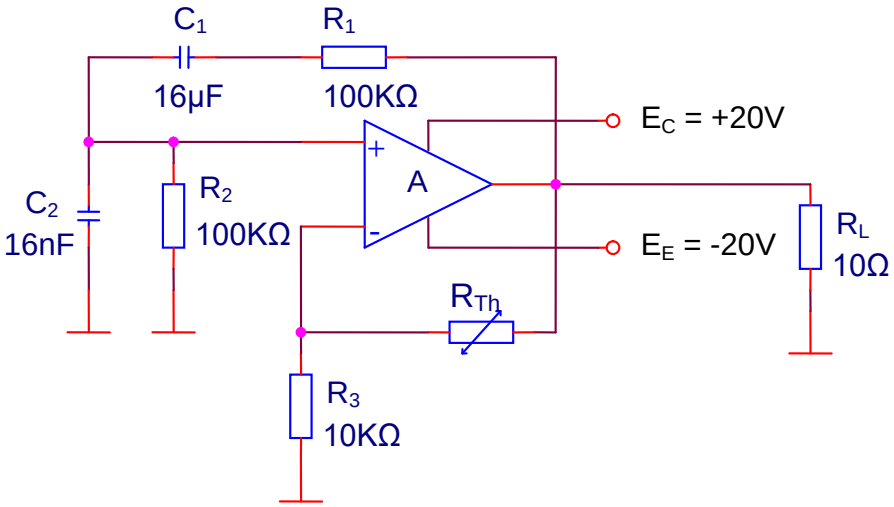
According to SCTC:

$$\frac{1}{f_i} = \frac{1}{f_{i1}} + \frac{1}{f_{i2}} + \frac{1}{f_{i3}} \Rightarrow f_i \cong 385{,}2KHz.$$

close to the value obtained at a)

2. (15p) The schematic below is a Wien oscillator using a class B final stage amplifier having: $A_u \rightarrow \infty$, $R_i \rightarrow \infty$, $R_o \rightarrow 0$. Find out:

a) f_o oscillating frequency,
b) V_0, when using the thermistor R_{Th};
c) P_0 (delivered to R_L)



Solution:

a) $f_o = \frac{1}{2 \cdot \pi \cdot \sqrt{R_1 R_2 C_1 C_2}} \cong 100Hz$

b) $A = 1 + R_{Th}/R_3$, and at f_0: $|\beta| = 1/3$.

From $|A||\beta| = 1 \Rightarrow R_{Th} = 20K\Omega$ obtained for $U_{Th} = 10V$.
Feedback topology is series-shunt, actually a voltage divider including R_{Th}, so:

$$u_{Rth} = u_o \cdot \frac{R_{Th}}{R_{Th} + R_3} = \frac{2}{3} \cdot u_o \Rightarrow u_o = 1{,}5 \cdot u_{Rth} = 15V_{ef}$$

$$u_{om} = \sqrt{2} \cdot 15V_{vv}$$

c)

$$P_o = \frac{u_{om}^{\ 2}}{2 \cdot R_L} = 22{,}5W$$

DIGITAL INTEGRATED CIRCUITS

3. Implement a modulo p counter.

Let p=51. The number of flip-flops needed to implement it is *n*, where $2^{n-1}<51<2^n$. $n=6$ ($32<51<64$)

A modulo p = 51 means resetting the counter after the 51st clock tick. This is done by identifying the state 51 with a circuit (an AND/NAND gate) and clear the counter by activating /CLR.
The truth table for the modulo 51 counter is shown below.

Table 11.1 Truth table for a modulo p=51 counter

Clock tick	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0
0	0	0	0	0	0	**0**
1	0	0	0	0	0	**1**
.						
50	1	1	0	0	1	**0**
51 (0)	$1 \rightarrow 0$	$1 \rightarrow 0$	**0**	**0**	$1 \rightarrow 0$	$1 \rightarrow 0$

A 4 input NAND gate is needed to detect the 51 state.

p = 51 = 1*32 + 1*16 + 0*8 + 0*4 +1*2 + 1*1

The inputs of the gate are connected to the Q_5, Q_4, Q_1, Q_0 outputs which are „1” logic only when the state 51 is detected. At that moment input /CLR is active (the output of the NAND gate is „0”only in this state) and clears the counter, so state 51 becomes state 0, in this way the number of distinct states of the counter is reduced to 51.

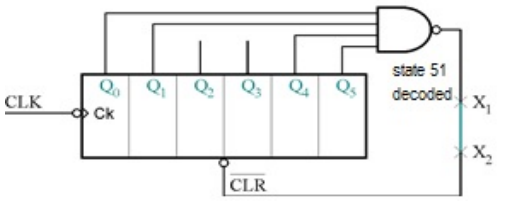


Fig 11.1 Decoding state 51

This schematic has an issue due to dispersion of the propagation times t_{CLR-Q}. The flip-flop with the shortest propagation time is clear first and its output Q (which is one of the inputs of the NAND gate) goes to "0". Thus, the gate output switches to "1" and interrupts the counter full reset process (other bistable will not be deleted).

To eliminate this disadvantage an /S-/R-flip-flop is used to hold the /CLR line active long enough time to clear all flip-flops but shorter than the clock pulse. The /S-/R-flip-flop is inserted between X1 and X2.

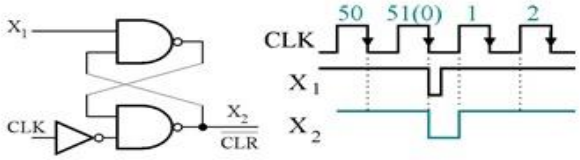


Fig. 11.2 Genereting a proper clear signal

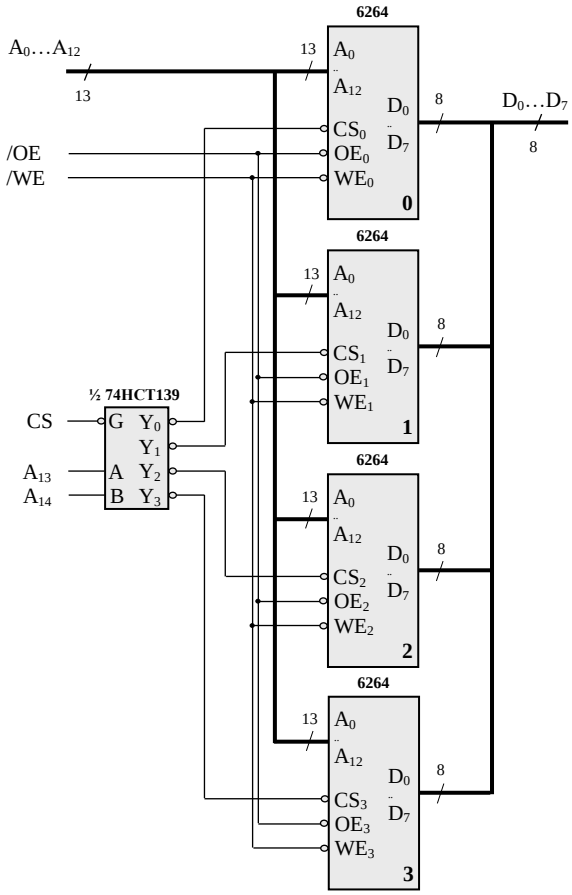
4. Using semiconductor memory SRAM 6264 (8k x 8 bit) and a minumum number of logic circuits implement a 32k x 8 bit memory.

First the number of circuits of type 6264 is determined.

$$N = \frac{32k\,x\,8bit}{8k\,x\,8bit} = 4\,.$$

The 8k memory has $2^3 \cdot 2^{10} = 2^{13}$ memory locations which can be acces by using 13 adress lines (A_0, …, A_{12}). The 32k memory has $2^5 \cdot 2^{10} = 2^{15}$ memory locations which can be acces by using 15 adress lines (A_0, …, A_{14}). The aditional adresses A_{14} and A_{13} decoded with a 2:4 DCD are used to enable the 4 semiconductot memories of type 6264 acording to the table below.

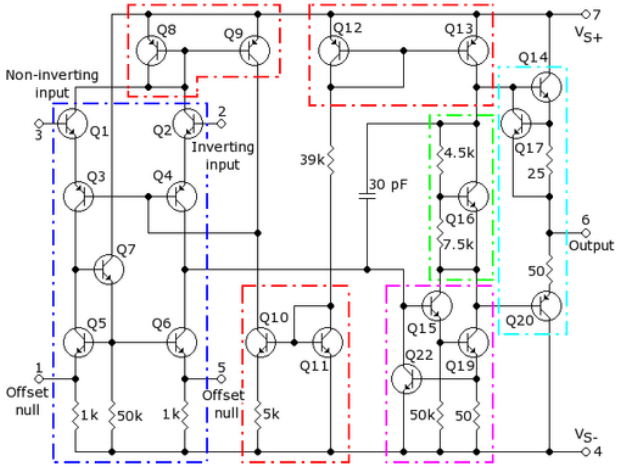
Fig 12.1 A 32k x 8 bit memory buil with 4 ICs 6264



A_{14}	A_{13}	$A_{12}-A_0$	Enabled Circuit	Enable conditions			
				$\overline{CE_0}$	$\overline{CE_1}$	$\overline{CE_2}$	$\overline{CE_3}$
0	0	X.....X	0	0	1	1	**1**
0	1	X.....X	1	1	0	1	**1**
1	0	X.....X	2	1	1	0	**1**
1	**1**	**X.....X**	**3**	**1**	**1**	**1**	**0**

Table 12.1 Truth table for the 32kx8bit memory

5. Name the building blocks inside the op amp shown in the figure.



Solution

1. At the left-hand side of the figure, the first block is a differential input stage with emitter followers (Ql and Q2) driving common-base stages (Q3 and Q4).
The transistors Q5 and Q6 form an active load for Q3 and Q4.
Q7, Q5, Q6 and their emitter resistances form a current mirror with degeneration.
The two pairs of transistors shown at the top of the schematic are simple current mirrors (Q8 and Q9, Q12 and Q13).
At the bottom is a Widlar current source (built with Q10, Q11, and the 5 kΩ resistor).
Transistors Q15, Q19 and Q22 operate as a class A gain stage. The stage consists of two NPN transistors in a Darlington configuration (Q15 and Q19).
Transistor Q16 and its base resistors is the V_{be} multiplier voltage source.
Transistors Q14, Q20 form the class AB push-pull emitter follower output stage.

6. A bandgap reference is shown in the figure. T1 and T2 are identical, the ratio of R_{c1} to R_{c2} is 2: $R_{c1}/R_{c2} = 2$, $R_1 = 2.6\ K\Omega$.

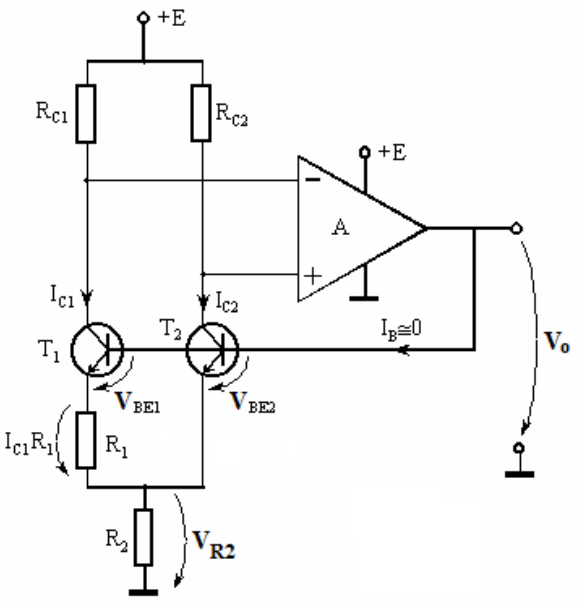
a). Determine the expression of the output voltage V_o and prove that it is possible to have a bandgap voltage reference.

b). Calculate the value of the output voltage.

c). Calculate the value of the curents I_{c1} and I_{c2}.

You have: ln2 = 0.693 ; ln5 = 1.6 ; ln10=2.3 ;

V_T= 26mV at 300 K.



Solution

a). In order to be a band-gap referenced circuit, the output voltage has the general form :

$$V_o = V_{BE} + NV_T \qquad (1)$$

In our case : $$V_o = V_{BE2} + R_2(I_{c1} + I_{c2}) \qquad (2)$$

We have to show that $(I_{c1} + I_{c2})$ is direct proportional to V_T.

First, we consider an ideal op amp. This means that $V_- = V_+$ and I_{c2} flows through R_{c2} and

$$R_{c2}I_{c2} = R_{c1}I_{c1} \quad \Rightarrow \frac{I_{c2}}{I_{c1}} = \frac{R_{c1}}{R_{c2}} \Rightarrow \quad \frac{I_{c2}}{I_{c1}} = 2 \quad (3)$$

KCL : $V_{BE1} + R_1 I_{c1} = V_{BE2} \qquad (4)$

$$\Rightarrow V_{BE2} - V_{BE1} = R_1 I_{c1} \quad \Rightarrow V_T \ln \frac{I_{c2}}{I_{s2}} \frac{I_{s1}}{I_{c1}} = R_1 I_{c1} \quad \Rightarrow I_{c1} \overset{(I_{s1}=I_{s2})}{=} \frac{V_T}{R_1} \ln \frac{I_{c2}}{I_{c1}} \overset{(3)}{=} \frac{V_T}{R_1} \ln 2 \qquad (5)$$

$$\overset{(2),(3),(5)}{\Rightarrow} V_o = V_{BE2} + 3 \cdot R_2 \frac{V_T}{R_1} \ln 2 \qquad (6)$$

V_o will be compensated if : $3 \cdot R_2 \dfrac{\ln 2}{R_1} = N = 23$

$$\Rightarrow R_2 = \frac{23 \cdot R_1}{3 \cdot \ln 2} = \frac{23 \cdot 2.6 \cdot 10^3}{3 \cdot 0.693} \approx 28.7 K\Omega$$

b). Thereby, if R2 = 28.7 KΩ, we have a band-gap refferenced circuit and the output voltage is :

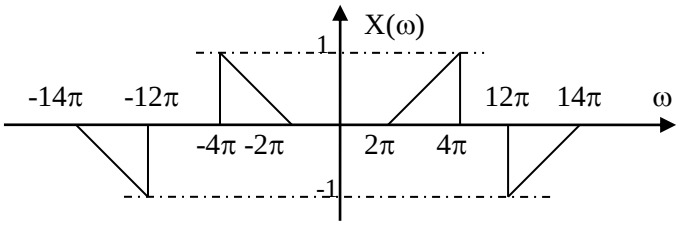
$$V_o = V_{BE} + NV_T \approx 0.6V + 23 \cdot 26 \cdot 10^{-3} \approx 1.2V$$

c). $$I_{c1} \overset{(5)}{=} \frac{V_T}{R_1} \ln 2 = \frac{26 \cdot 10^{-3} \cdot 0.693}{2.6 \cdot 10^{-3}} = 6.93 \cdot 10^{-6} A$$

$$I_{c2} = 2I_{c1} = 13.86 \cdot 10^{-6} A$$

SIGNAL PROCESSING

7. Consider the signal $x(t)$ with the spectrum below



What is the minimum sampling frequency $f_{s\min}$ according to the sampling theorem?

Answer

$$f_M = \frac{14\pi\,[rad/s]}{2\pi\,[rad]} = 7\ Hz$$

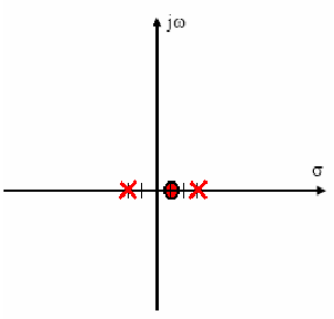
$$f_{s_{\min}} = 2\,f_m = 2\cdot 7\ Hz = 14\ Hz$$

8. Consider the system with the transfer function $H(s) = \dfrac{s-1}{(s+2)(s-3)}$.

Sketch its pole/zero plot.

Answer

$$X(s) = \frac{s-1}{(s+2)(s-3)}$$



x- pole
o - zero

ELECTRONIC INSTRUMENTATION

9. The 50 ns rise time of a square wave (t_{ri}) read on the screen of an oscilloscope (t_{ro}) is 60 ns. Determine the oscilloscope's bandwidth! Round it off to the nearest standard value (10, 20, 35, 40, 50, 60, 75, 100, 150, 250, 300, 500 MHz)!

Solution

Using the equation $t_{ro}^2 = t_{ri}^2 + t_r^2$, the rise time of the oscilloscope is found to be

$$\sqrt{3600-2500} = \sqrt{1100} = 33.16ns$$

The bandwidth is

$$B = \frac{350}{t_r} = \frac{350}{33.16} = 10.55 MHz$$

The nearest standard value is 10 MHz.

10. An universal counter displays 100.100 kHz when measuring the frequency of an input signal. Determine the quantization error in Hz, % and ppm! (remember, "." is the decimal point)

Solution

The quantization error is 1 Hz (one least significant digit)

or, in percent

1 Hz / 100100 Hz × 100 = 0.001%

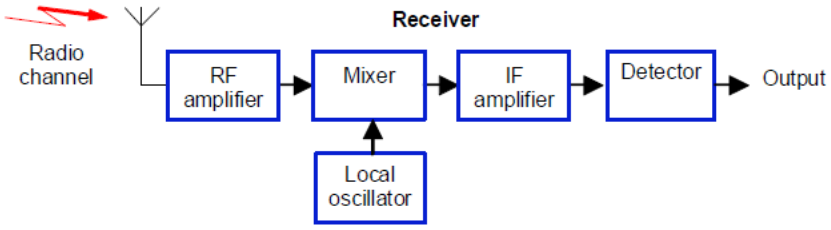
or, in ppm

1 Hz / 100100 Hz × 1,000,000 = 10 ppm.

RADIOCOMMUNICATIONS – S16

1. Draw and explain the main blocks of a radio receiver.
Course nb.1 slide 12.
Site address: https://intranet.etc.upt.ro/~RADIOCOM/

Answer:
Receiver operations include amplification to compensate for transmission loss, and demodulation and decoding to reverse the signal-processing performed at the transmitter. Filtering is another important function at the receiver.



The receiver block incorporates many amplifier and processing stages, and one of the most important is the oscillator stage.
The receiver oscillator is called the local oscillator as it produces a local carrier within the receiver which allows the incoming carrier from the transmitter to be down converted for easier processing within the receiver.

2. What wavelength corresponds to a frequency of 600 MHz?
Course nb.2 slide 45.
Site address: https://intranet.etc.upt.ro/~RADIOCOM/

Answer:
$\lambda = c/f = (3x10^8 m/s)/(6x10^8 Hz) = 0.5$ m

3. What are the radiation regions of an antenna?
Course nb.3 slide 36-39.
Site address: https://intranet.etc.upt.ro/~RADIOCOM/

Answer:
The antenna radiation field is divided into
- reactive near-field (objects within this region will result in coupling with the antenna and distortion of the ultimate far-field antenna pattern),
- radiating near-field (transition region),
- far-field (the gain of the antenna is a function only of angle).

4. Describe the directivity of a half-wave dipole antenna.
Course nb.4 slide 35-36.
Site address: https://intranet.etc.upt.ro/~RADIOCOM/

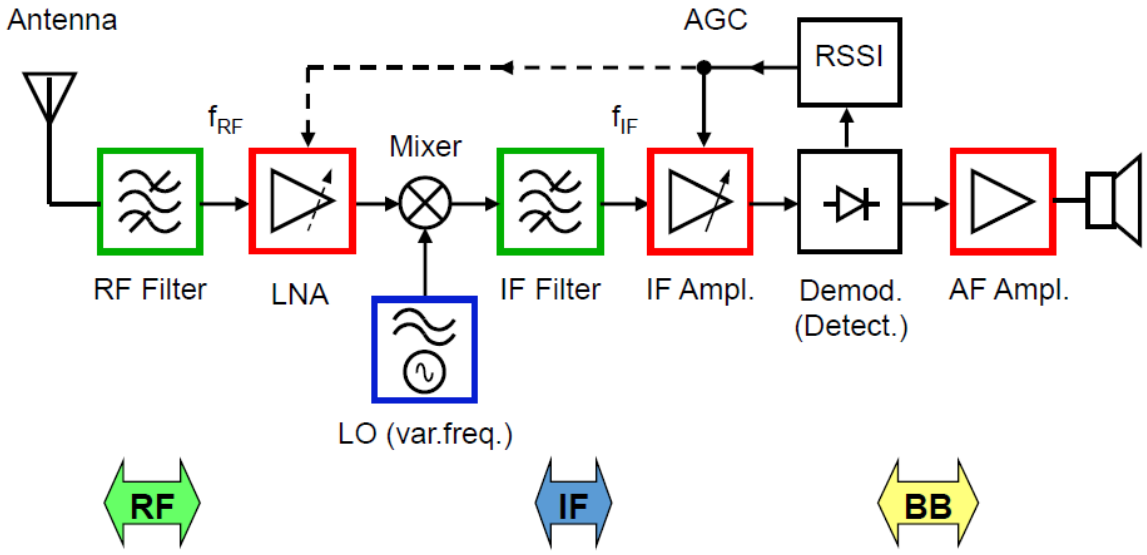
Answer:
A half-wave dipole has an antenna gain of 1.64 or $G = 2.15$ dBi.
It has an omnidirectional pattern in the H-plane.
In E-plane the directivity is bidirectional.

5. What represents the array factor?
Course nb.5 slide 15-16.
Site address: https://intranet.etc.upt.ro/~RADIOCOM/

Answer:
An array antenna is radiating system comprised of a number of identical radiating elements in a regular arrangement and excited to obtain a prescribed radiation pattern.
The array factor is defined as the cumulative contribution of all the isotropic radiating elements of an array antenna at an arbitrary far-field point.

6. Draw and explain the main blocks of a superheterodyne receiver.
Course nb.6 slide 9-11.
Site address: https://intranet.etc.upt.ro/~RADIOCOM/

Answer:

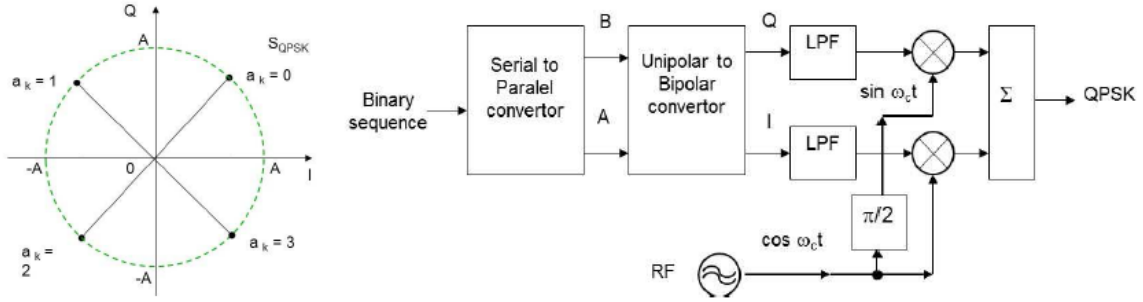


This is the most popular architecture used in communication receivers.
It is based on the heterodyne process of mixing an incoming signal with an offset frequency local oscillator (LO) in a nonlinear device to generate an intermediate frequency (IF) signal.

The nonlinear device executing the heterodyne process is called a frequency mixer or frequency converter.
In a superheterodyne transceiver, the frequency translation processes may be performed more than once and thus it may have multiple intermediate frequencies and multiple IF blocks.

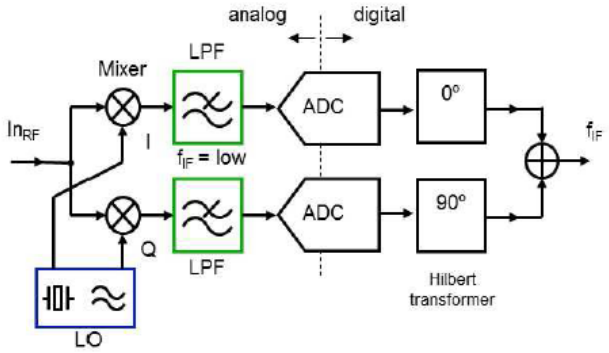
7. Draw and explain the QPSK modulator.
Course nb.7 slide 33-34.
Site address: https://intranet.etc.upt.ro/~RADIOCOM/

Answer:
Quadrature PSK is the most common type of PSK modulation. The QPSK phasor has a constellation with four states. The phase shift between two consecutive states is 90°. The modulation is done with two bits per symbol.



8. Explain the image reject mixer with Hartley architecture.
Course nb.8 slide 17-23.
Site address: https://intranet.etc.upt.ro/~RADIOCOM/

Answer:
In case of image reject mixer with Hartley architecture, the RF signal in the downconversion is split into two components by using two matched mixers and quadrature LO signals.
The resulting IF signals, namely in phase (I) and quadrature phase (Q), are then lowpass-filtered and after one is phase-shifted by 90°, the IF signals are combined.
In this process, depending on the IF path that is subjected to the 90° phase-shifter, either the image band or the receive band is cancelled after the summation of I and Q outputs.

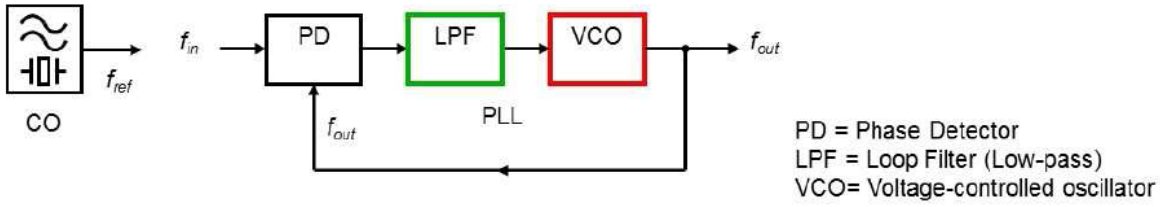


9. Define the receiver's selectivity.
Course nb.9 slide 19.
Site address: https://intranet.etc.upt.ro/~RADIOCOM/

Answer:
A receiver's selectivity performance is a measure of the ability to separate the desired band around the carrier, from unwanted interfering signals received at other frequencies.
This situation is most often characterized by a weak received desired signal in the presence of a strong adjacent or alternate band user.
Receiver selectivity may be defined also as the ability to reject unwanted signals on adjacent channel frequencies. This specification, ranging from 70 to 90 dB, is difficult to achieve.

10. Which are the major components of the PLL (Phase-locked loop) frequency synthesizer?
Course nb.10 slide 27-29.
Site address: https://intranet.etc.upt.ro/~RADIOCOM/

Answer:
A PLL is a circuit which causes a particular system to track with another one. More precisely, a PLL is a circuit synchronizing an output signal (generated by an oscillator) with a reference or input signal in frequency as well as in phase.
In the synchronized (often called locked) state the phase error between the oscillator's output signal and the reference signal is zero, or remains constant.
The basic blocks are a phase comparator, a filter, and a controlled oscillator. Even complex PLLs share this configuration.



1. Define the *total harmonic distortion* coefficient (*THD*) for a periodic signal *x(t)* and the *power factor* (*PF*) at a port with periodic voltage and current. Power factor formula for *sinusoida*l input voltage and nonlinear load.

The *total harmonic distortion coefficient* (THD) is defined as:

$$THD = \frac{rms\ \ value\ without\ \ \ fundamental}{rms\ \ \ fundamental} = \frac{\sqrt{X_0^2 + \frac{1}{2}\sum_{n=2}^{\infty} X_n^2}}{\frac{X_1}{\sqrt{2}}}$$

where X_0 is the dc component and X_n are the amplitudes of harmonics.

The *power factor* (*PF*) is a *figure of merit* that measures how efficiently the energy is transmitted. It is defined as the ratio between average power and apparent power:

$$PF = \frac{P}{S} \cdot \frac{P}{V_{rms} \cdot I_{rms}} = \frac{\int_{t_0}^{t_0+T} v(t) \cdot i(t) dt}{\sqrt{\frac{1}{T}\int_{t_0}^{t_0+T} v(t)^2 dt} \cdot \sqrt{\frac{1}{T}\int_{t_0}^{t_0+T} i(t)^2 dt}} \qquad (1)$$

With a *sinusoidal voltage,* current harmonics do not lead to average power but only the fundamental. However, current harmonics increase the rms current and hence they decrease the power factor.

As with a sinusoidal voltage we have $P = \frac{1}{2} V_1 I_1 \cos(\varphi_1 - \theta_1)$; $V_{rms} = \frac{V_1}{\sqrt{2}}$;

$I_{rms} = \sqrt{I_0^2 + \frac{1}{2}\sum_{n=2}^{\infty} I_n^2}$,

from (1) it results that

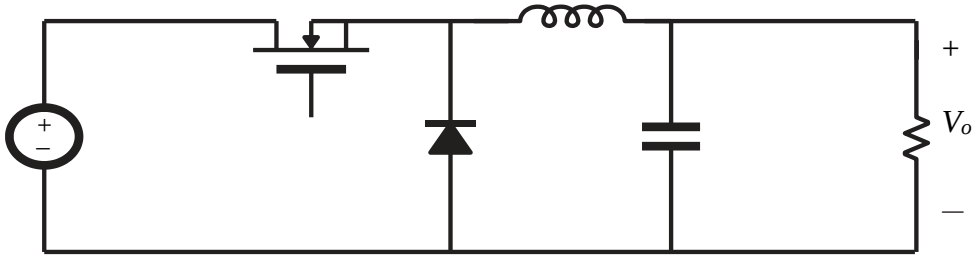
$$PF = \frac{\frac{I_1}{\sqrt{2}}}{\sqrt{I_0^2 + \frac{1}{2}\sum_{n=2}^{\infty} I_n^2}} \cdot \cos(\varphi_1 - \theta_1) = K_{di} \cdot K_\theta$$

where

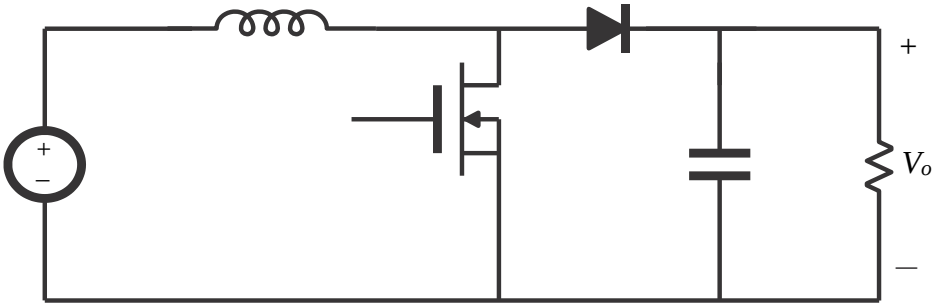
$$K_{di} = \frac{\frac{I_1}{\sqrt{2}}}{\sqrt{I_0^2 + \frac{1}{2}\sum_{n=2}^{\infty} I_n^2}} = \text{current distortion factor}$$

$$K_\theta = \cos(\varphi_1 - \theta_1) = \text{displacement factor}$$

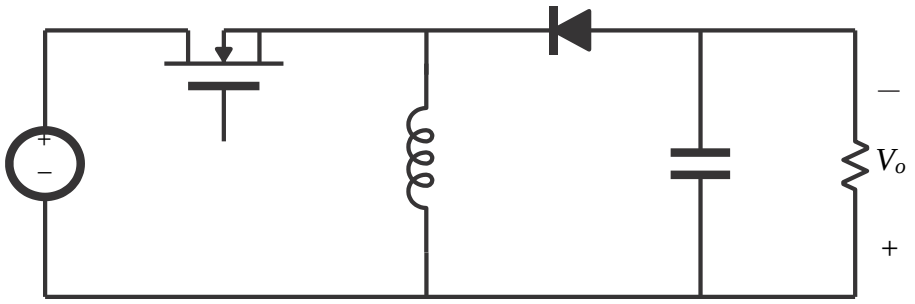
2. The four *basic dc-dc nonisolated ideal converters*: buck, boost, buck-boost, Ćuk: schematics with MOS transistors and diodes and their static conversion ratio M in terms of transistor duty cycle D. Also indicate the output voltage polarity for each topology.



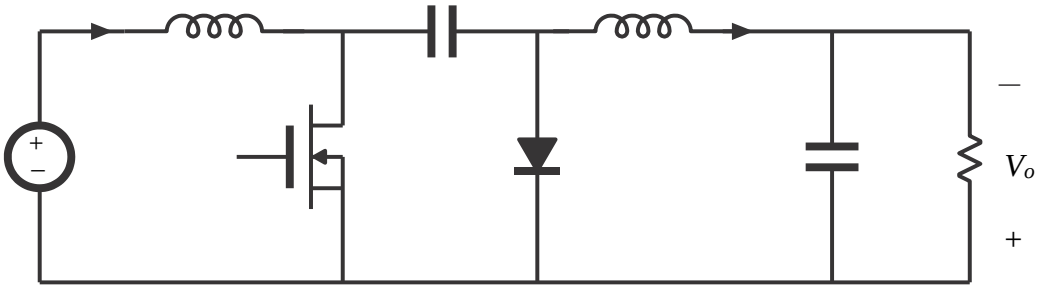
Buck converter. $M(D) = D$.



Boost converter. $M(D) = \dfrac{1}{1-D}$.

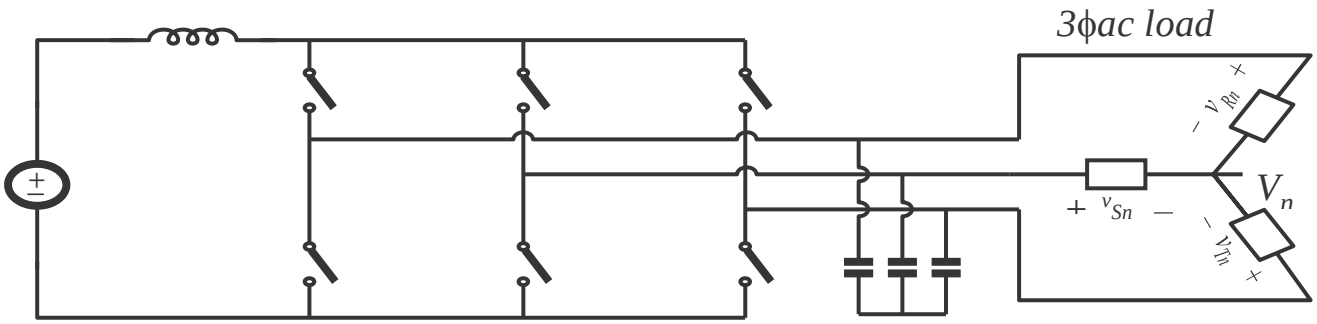


Buck-Boost converter. $M(D) = \dfrac{D}{1-D}$.

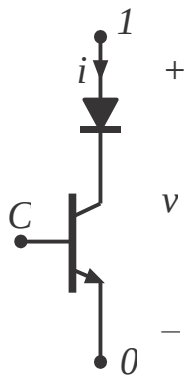


Ćuk converter. $M(D) = \dfrac{D}{1-D}$.

3. The *three phase current source inverter* – schematics, characteristic nature, practical switch implementation.



Exhibits a *boost-type* conversion characteristic. The switches are *current unidirectional* (voltage bidirectional) two quadrant switches, such as below:



4. Derive the *CCM operation condition* for an ideal *buck-boost* converter and provide the *unconditioned* CCM operation (at any duty cycle) condition.

Generally speaking, the *diode* is responsible for DCM operation as it is a *current unidirectional* device. The CCM operation imposes that all semiconductors switch synchronous. This means that the diode never ceases to conduct during the second topological state, till the transistor is switched on again. Consequently, the current through the diode in the second topological state has to stay positive or, equivalently, the minimum diode current has to be positive. Hence:

$$I_{D\min} \geq 0 \tag{1}$$

Denoting the dc inductor current by I_L and its peak to peak ripple by ΔI_L, the minimum diode current can be expressed as:

$$I_{D\min} = I_L - \frac{1}{2}\Delta I_L \tag{2}$$

and the condition becomes

$$I_L \geq \frac{1}{2}\Delta I_L \tag{3}$$

The dc inductor current in a *buck-boost* topology (for schematic see problem 1) is the sum of the dc input current and dc output current:

$$I_L = I_g + I_o = \frac{D}{1-D} I_o + I_o = \frac{I_o}{1-D} = \frac{\frac{V_o}{R}}{1-D} = \frac{D}{(1-D)^2} \frac{V_g}{R} \tag{4}$$

In deriving the value for I_L it was taken into account that the static conversion ratio M for a buck-boost equals $\frac{D}{1-D}$ and the ratio between the input current I_g and output current I_o equals the static conversion ratio M .

The inductor current peak to peak ripple can be derived from the first topological state as:

$$\Delta I_L = \frac{DV_g}{Lf_s} \tag{5}$$

Substituting (4) and (5) in (3) results in:

$$\frac{D}{(1-D)^2} \frac{V_g}{R} \geq \frac{DV_g}{Lf_s} \tag{6}$$

After some simple algebra, from (6) it follows that the CCM operating condition is:

$$\frac{2Lf_s}{R} \geq (1-D)^2 \tag{7}$$

Unconditioned CCM operation is obtained when inequality (7) is valid at *any* duty cycle. This occurs if the left hand side in (7) is higher than the maximum value of the right hand side. Obviously, the maximum right hand side is obtained when D=0 and hence the unconditioned CCM operation requires

$$\frac{2Lf_s}{R} \geq 1 \tag{8}$$

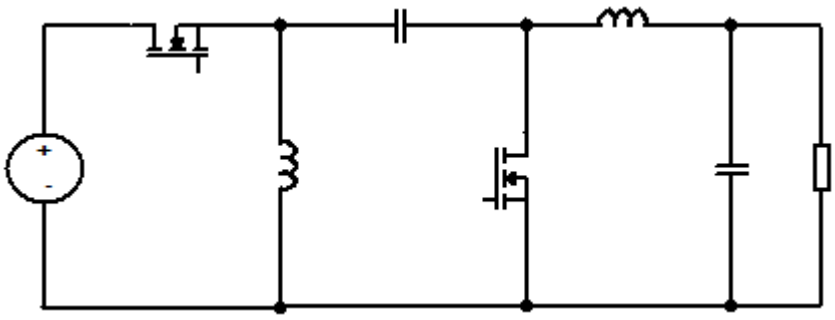
5. Explain when synchronous rectification is suitable, what synchronous rectification is and enumerate at least two of its advantages. Draw the schematic of a *synchronous Zeta* converter.

Synchronous rectification is used in *high current* applications, when the conduction losses in the diodes are high because of the high currents that flow through them. Synchronous rectification means to replace the diode by a MOS transistor, as the latter exhibits much lower losses due to its low on resistance. The MOS is connected such that *its internal diode to play the role and be positioned the same as the diode that is replaced*.

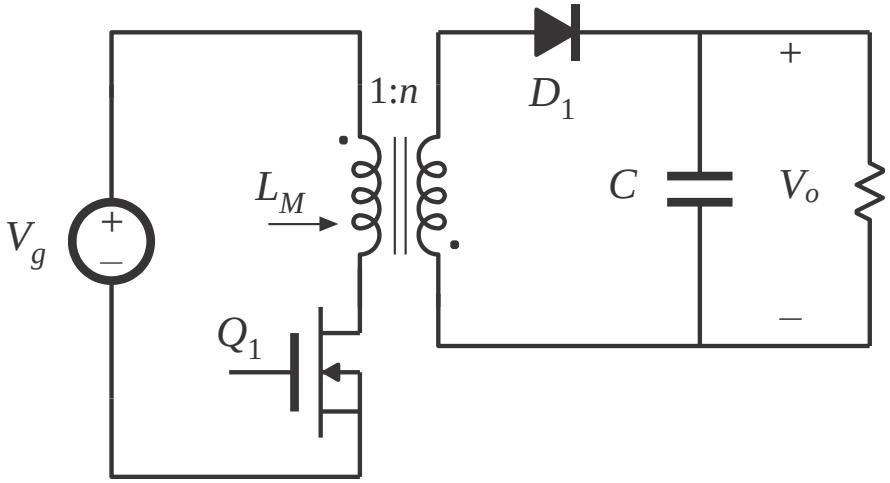
Advantages of synchronous rectification are:

- *High efficiency* because the conduction losses are reduced.
- *Absence of discontinuous conduction mode*, because the diodes are the cause of DCM occurrence and in synchronous rectification they are missing.

The synchronous Zeta converter is presented below



6. The *flyback* converter: schematics, static conversion ratio, applications, advantages and limitations.



$$M(D) = n\frac{D}{1-D} = n\frac{D}{D'}$$

- Widely used in *low power* and/or *high voltage* applications

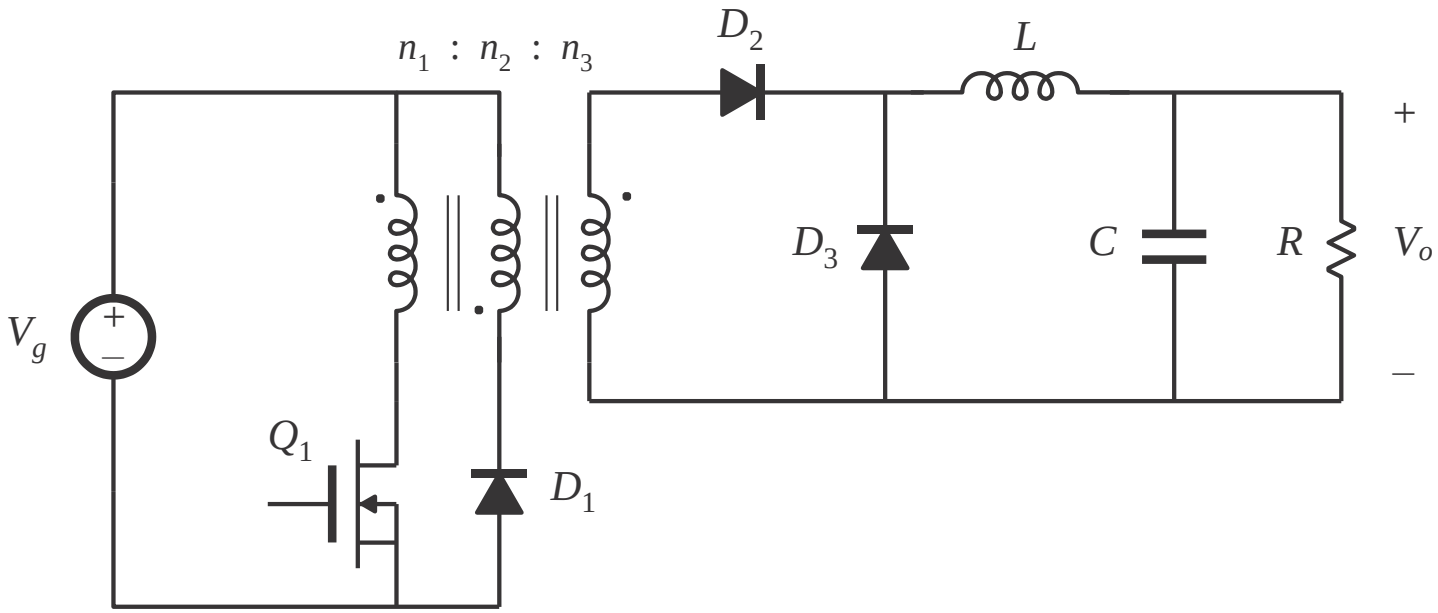
Advantages

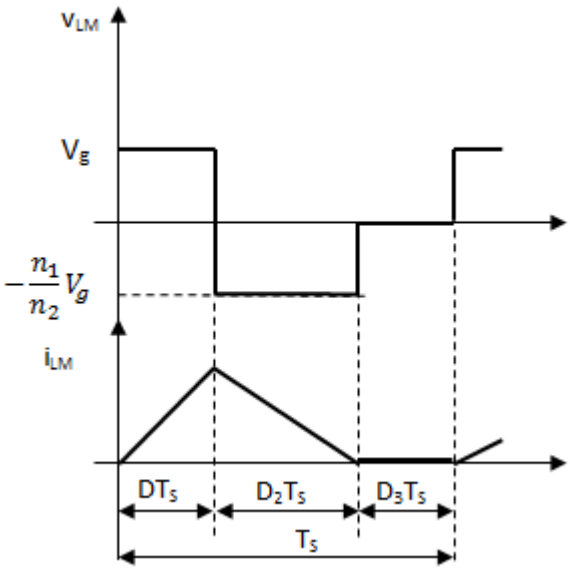
- Low parts count
- Multiple outputs are easily obtained, with minimum additional parts
- Often operated in discontinuous conduction mode

Limitations

- Cross regulation is inferior to buck-derived isolated converters
- Cannot be used at high power levels as it requires bulky magnetic cores

7. The classical single-transistor *forward* converter: schematics, maximum duty cycle.





From magnetizing inductor volt-second balance we get that

$$DV_g + (D_2)(-\frac{n_1}{n_2}V_g) + D_3 \cdot 0 = 0$$

Solve for D_2:

$$D_2 = \frac{n_2}{n_1}D$$

On the other side, D_3 cannot be negative. But $D_3 = 1 - D_2 - D$. Hence, using the value for D_2 previously obtained, it follows that:

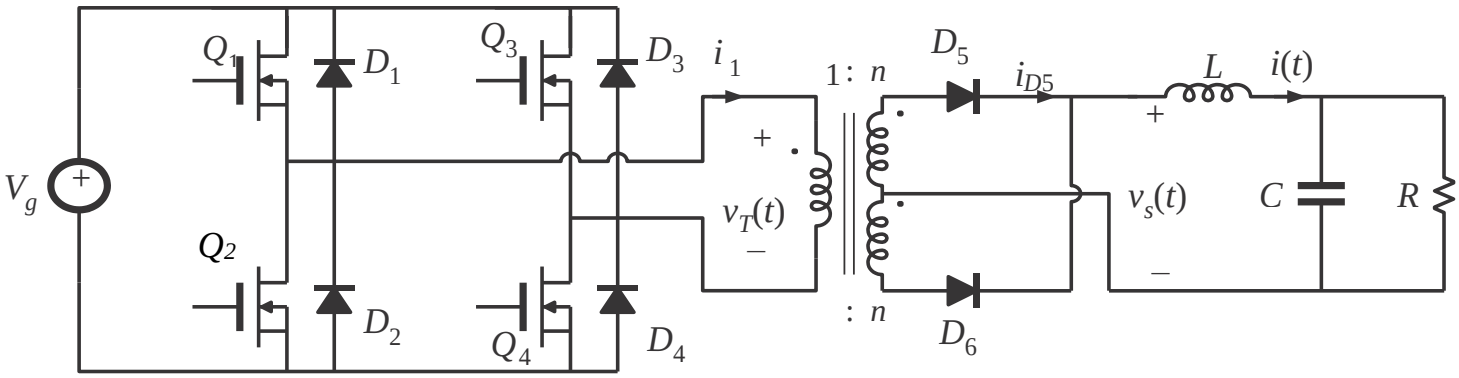
$$1 - \frac{n_2}{n_1}D - D \geq 0\,,$$

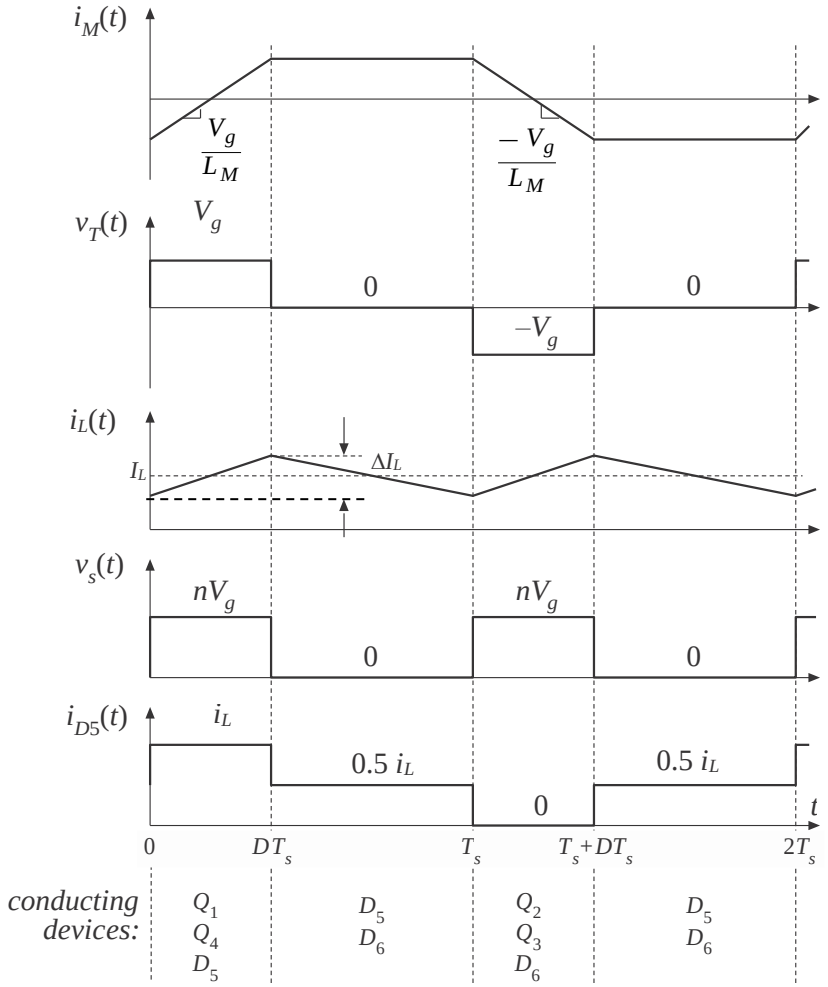
finally resulting in

$$D \leq \frac{1}{1+\frac{n_2}{n_1}}$$

Note. If the final result is provided without proof the answer will also be accepted.

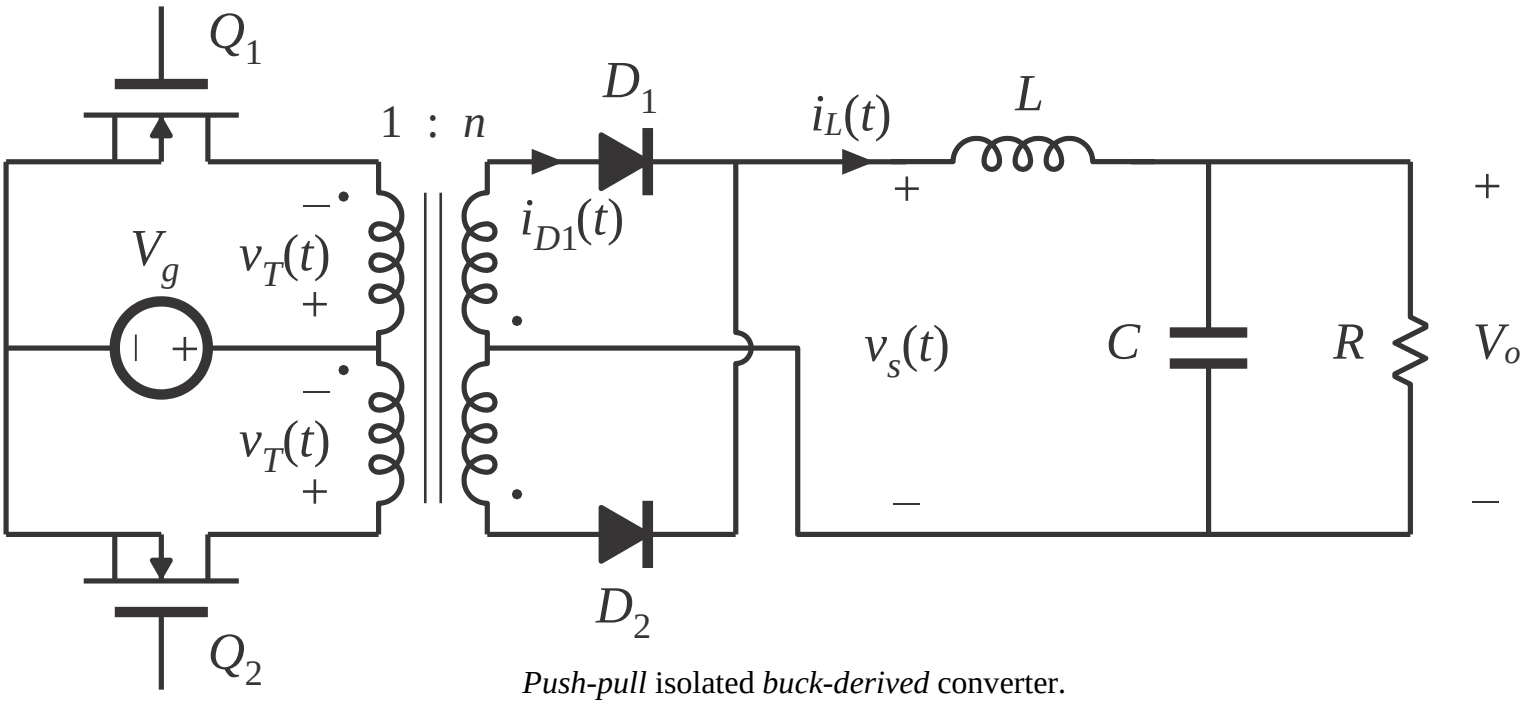
8. The *full-bridge* isolated *buck* converter: schematics, main waveforms (at least magnetizing current, transformer primary voltage, output inductor current and output diodes current), solutions for preventing core saturation.





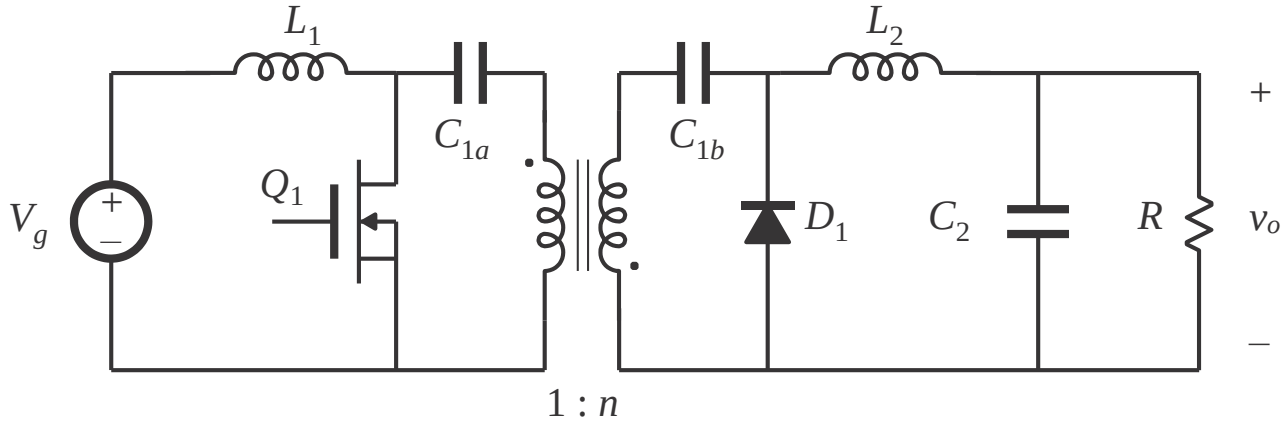
Saturation can be prevented by placing a *capacitor* in series with primary or by use of *current mode control.*

9. *Push-pull isolated buck* and *isolated Ćuk* converters: schematics, type of control, considerations regarding transformer magnetizing current.



Push-pull isolated *buck-derived* converter.

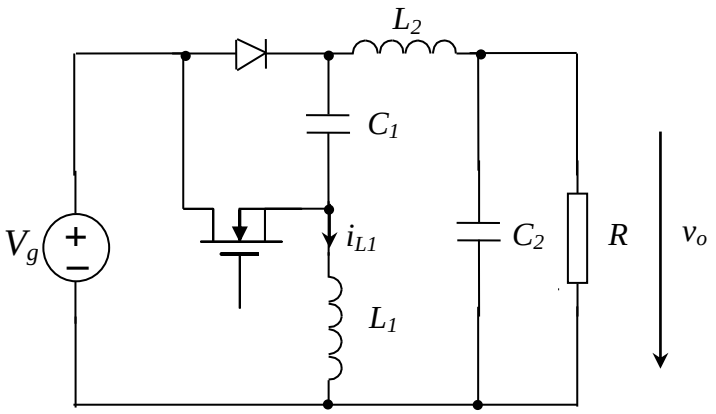
Current programmed control can be used to mitigate transformer saturation problems. Duty cycle control *not* recommended.



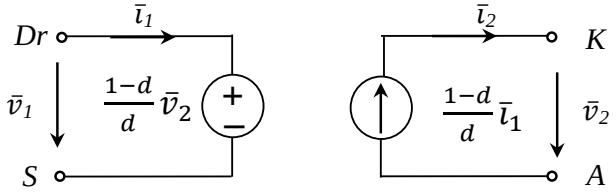
Ćuk isolated buck-derived converter

Capacitors C_{1a}, C_{1b} ensure that *no dc voltage is applied to transformer primary* or secondary windings. Transformer operates in conventional manner, with *small magnetizing current* and negligible energy storage within the magnetizing inductance. The *dc magnetizing current is zero* because of the series capacitors, which is a significant advantage.

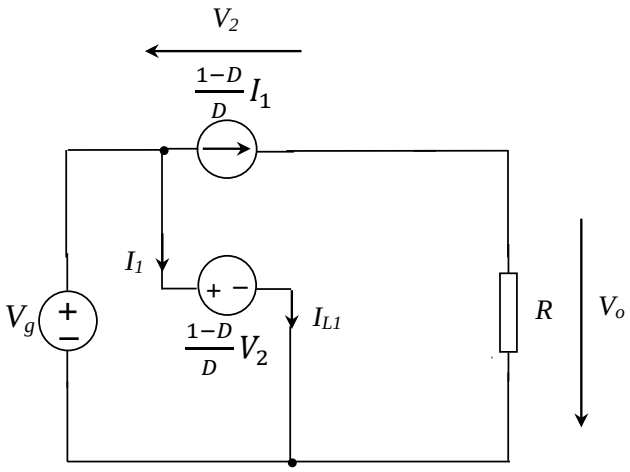
10. Given the CCM operated converter below, the transistor duty cycle is *D*. Find the static conversion ratio *M* in terms of duty cycle *D* using the *PWM switch large signal model*.



The large signal dynamic model of the PWM switch is represented below, where *d* is the *continuous duty cycle*, *Dr* and *S* represent the drain and the source terminals respectively and *A* și *K* refer to the diode anode and cathode respectively.



This averaged model will substitute the transistor and the diode in the original converter. Additionally, in *steady state the averaged model is a dc one* and hence *d*=*D*=constant, the inductors are short circuits and the capacitors are open circuits. All magnitudes are dc, denoted by capitals. The steady state averaged schematic is depicted below.



From the input loop we observe that

$$V_g = \frac{1-D}{D}V_2 \quad (1)$$

and the outer loop provides

$$V_o = V_2 + V_g \quad (2)$$

Substituting V_2 from (1) in (2) results in

$$V_o = \frac{1}{1-D}V_g \quad (3)$$

Hence

$$M = \frac{1}{1-D} \quad (5)$$

the converter being of *step-up* type.

ELECTRONIC EQUIPMENT TESTING – S18

1. Test levels: definition and description of each level's characteristics

There are three levels of test:

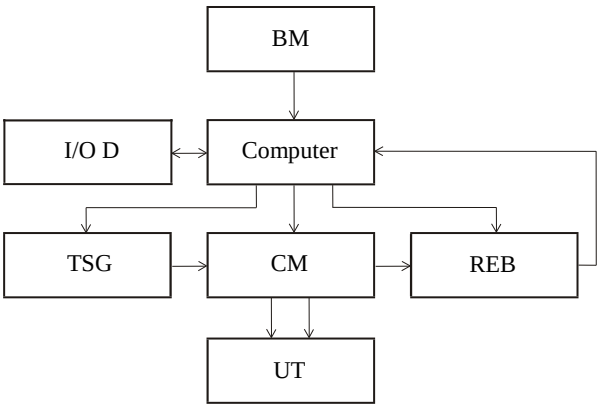
- *electronic component (including circuit board),*
- *electronic board (equipped circuit board - components),*
- *equipment.*

a) failed test at the component level – the component should not be mounted on the circuit board, economically has been proven that this test (also done by the producer) should be repeated by the user

b) can be done through "nails bed testing" (complicated and costly for realizing the test equipment) or through "test stimulus generation" (simple connection, but costly for implementing the test program)

c) depends on the equipment: normally involves broken connections between functionally correct boards. Can involve some more sophisticated equipment, such as the signature analyzer.

2. Architecture of an automatic test equipment. Characteristics of each block's functionality.



UT – unit under test
TSG – test signal generator
REB – responses evaluation block
CM – connection matrix
BM – back-up (external) memory
I/O D – Input/Output Devices

3. Principles of the signature analyzer

The signature analyzer is based on the principle of data information flow compression. The long data sequences are acquired from the tested board/equipment and compressed into fixed-length information, called "signature". The signature should be easy to be recognized, easy to be interpreted by comparing it with a control signature that corresponds to the correct functioning.
According to how the data flow is collected, the signature analyzer can be: serial or parallel.
The heart of the signature analyzer is a Pseudo-Random Sequence Generator, that performs data compression. The signature is provided as a fixed length information, on 16 bits, decoded into groups of 4 bits, displayed as alphanumeric characters on 7 segment LEDs. It avoids using small alphabet letters (b, c, d) and ambiguous capital letters (B, D, G, I), using instead letters like H, P, T, U.
The signature should be simple to be recognized, un-ambiguous and stable.
The signature analyzer should have the auto-test facility, in order to avoid wrong decisions.

4. Principles of testing the static parameters of a digital integrated circuit

The static parameters of an IC are:
- *Input and output voltages*
- *Input and output currents*

They are stable during the test. A time should be given from powering the IC, in order to allow stabilisation of the transition factors.
Test should be carried out under the less favourable conditions: minimum power supply value, maximum circuit's charge, etc.
The Test Signal Generator is formed by a number of Programmable Voltage Sources (PVS) and Programmable Constant Current Generators (PCCG).
The Responses Evaluation Block is a simple measuring instrument.
The Connection Matrix is formed by a number of relays or commuting transistors.

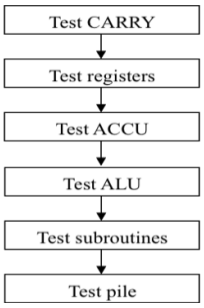
5. Principles of testing the dynamic parameters of a digital integrated circuit

The dynamic parameters of an IC are:
- *the transition times:* t_{tLH}, t_{tHL}
- *the propagation times:* t_{pLH}, t_{pHL}

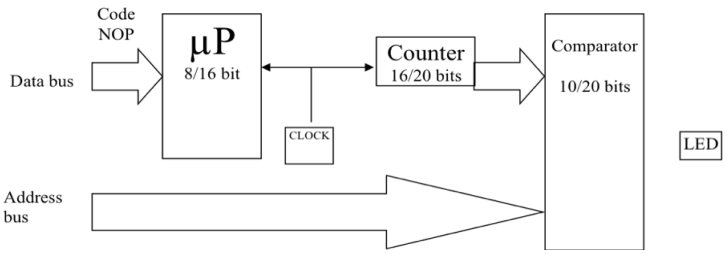
Those parameters might be defined by fixed or percentage thresholds. The realisation of the testing structure depends on that definition.
The evaluation should be done in the worst functional case: power supply, charge, etc
The Test Signal Generator uses digital programmable pulse generators: fronts, length, amplitude, polarity, filling factor, etc
The Responses Evaluation Block is typically formed by a counter, with "start" and "stop" commanded by the discriminated fronts of the tested parameter.

6. Principles of the modular activation method for processors' functional tests

The processor is divided on hierarchical levels (both functional and hardware).
The test is done based on a self-test program.
The program starts with the basic level
Each tested level can be used for testing superior levels
A possible testing strategy:



In order to start, a minimum level of components and functions should be correct! - KERNEL
The kernel should include: initialization circuits, program counter, address bus, data bus, instruction decoder, clock circuit
The hardware test of the kernel might be done through the following strategy:



If the kernel test is passed, the following circuits are functionally corrects:

- *Clock circuit*
- *Initialization circuit*
- *Program counter*
- *Address bus*
- *Data bus – partially*
- *Instruction decoder – partially*
- *Instruction register – partially*

7. Principles of the test stimulus vectors' generation

The test stimulus vectors are generated through algorithms that are describing the functions of the schema on a digital electronic board.
The main methods used are:

- *Single Path Activation Method*
- *Poage*
- *Poage McCluskey*

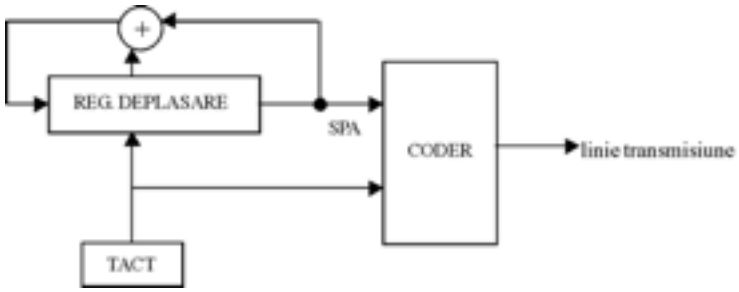
There are two basical principles:

- *forcing the complement of the tested error into the test node, then activation the propagation of the value in that node towards the observable output, where the received value is compared in order to take the decision: correct or erroneous board*
- *describing the functions on the board by using supplementary variables that are describing the functioning status of each line through their activation, then the condition to get complementary values at the output in case of "erroneous" or "correct" board is used in order to calculate the test stimulus vectors.*

8. Principles for testing the Bit Error Rate for a telecommunication digital network

The Bit Error Rate (BER) is the ratio between the number of error bits and the total number of transmitted bits
BER estimation can be done:
- *in-service*
- *out-of-service*

The test signal is a pseudorandom binary sequence, standardized through the 0.151 CCITT recommendation.
The principle of the test generator used at the transmission end is:



The problem is: avoiding the lock on 0 of the shift register.
At the reception end, there is a similar signal generator that provides the same sequence as at the emitter end, that is compared to the one received through the telecom network.
The problem is to ensure synchronization between the two generators.

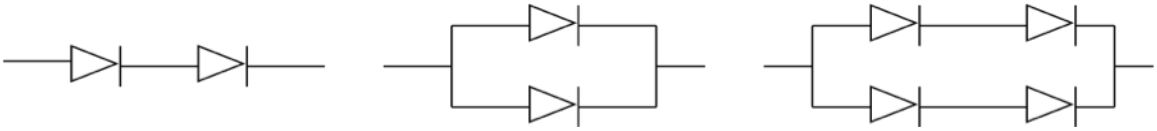
9. Principles for the realization of a fault tolerant system

Fault tolerance is an architectural attribute of a system, making possible for the system to function properly even when one or more faults appear in its structure.
Implementation is done through "redundancy", but the price to be paid is the high cost.
The use is in very critical applications: nuclear, military, aero-spatial, etc.
Fault = physical problem of one of the system's elements, taking to the permanent, temporary or intermittent erroneous function of the system
Error = symptom of a fault
The used strategies are:
- *Fault diagnosis and faulty elements replacement*
- *Fault masking*
- *Mixed strategies*

The used testing methods are:
- *Initial testing: before normal operation*
- *On-line testing: during normal operation*

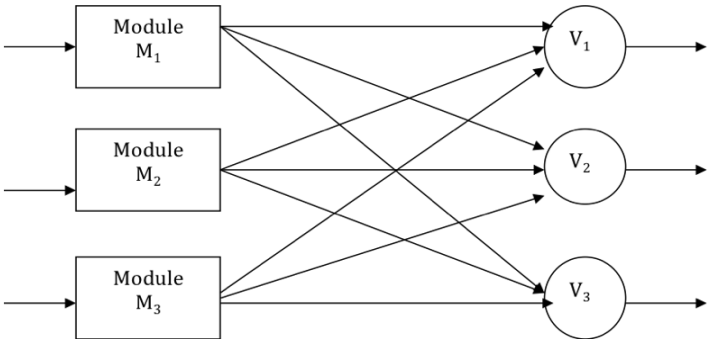
- *Off-line testing: for error detection and diagnosis*
- *Redundant modules testing: in order to see if the redundant modules are able to replace the modules that have been detected as faulty*

Redundancy is used in order to reconfigure the system: totally or partially.
A simple example of using redundancy in order to ensure protection to: shortcircuit, interruption, shortcircuit and interruption, respectively:

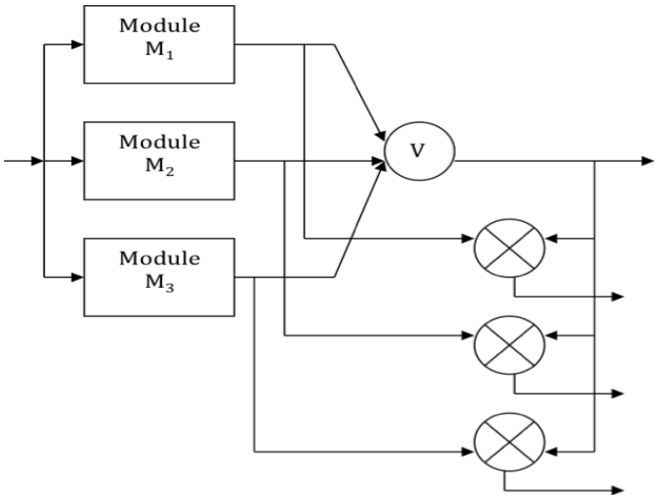


10. Principles for the detection of the faulty module in redundant electronic structures

The fault tolerant systems are implemented based on the use of majority logic redundant structures. The are using a multiple voter configuration:



In order to avoid that the error, once appeared in a module, be propagated into the system, the faulty module should be detected and replaced.



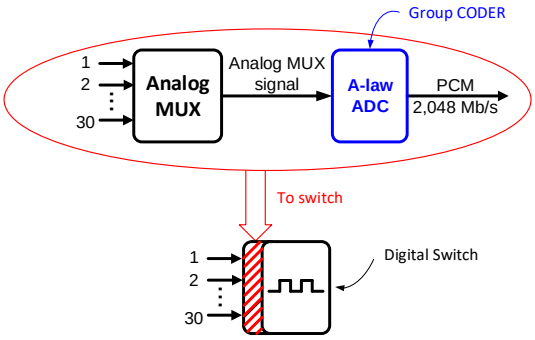
1. Compare the PCM codec solutions.

https://intranet.etc.upt.ro/~DIG_INT_NET/course/2015_2016/2_Line CODEC.pdf, 1, 2, 4

PCM Codec

- **Functions**
  1. Sampling
  2. Quantization
  3. Compression (A law or μ Law)
  4. Time division multiplexing (TDM)
- **Solutions**

1. Group CODEC



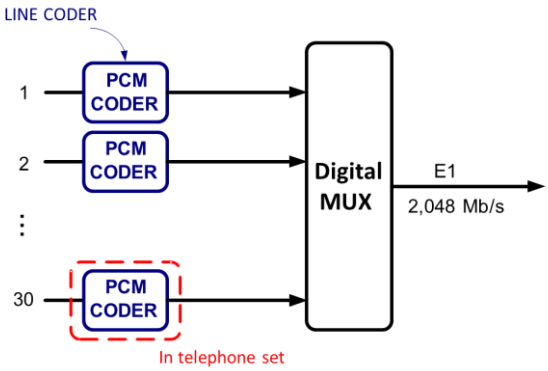
Sampling and TDM multiplexing of 30 analog channels followed by quantization and A-law compression.

Complexity: 1 Analog multiplexer (TDM) and 1 (high speed) codec for 30 channels.

Lower costs: less equipments + reuse existing analog subscriber loops.

Mixed analog/digital transmission: Signals are subject to interference and crosstalk in the analog domain.

2. Line CODEC



Sampling, qunantization, A-law compression for each of the 30 analog voice channels, followed by digital TDM.

Complexity: 30 individual (but slower) PCM codecs and 1 digital multiplexer (TDM).

Higher costs: more (cheap) equipments + require new 4 wires subscriber loops.

Full digital transmission: Signals are encoded as close as possible to the source → reduce the risk of interference and crosstalk.

2. Principle of positive justification.

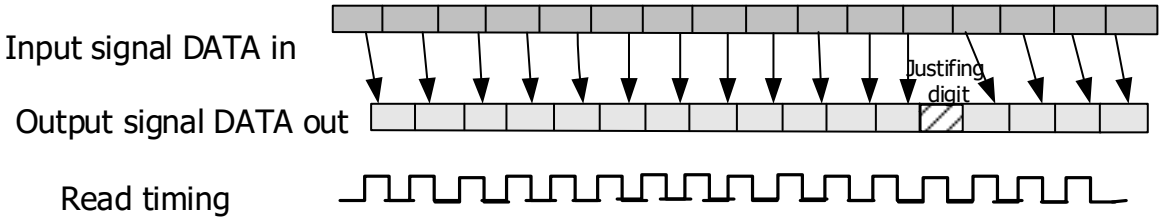
https://intranet.etc.upt.ro/~DIG_INT_NET/course/2015_2016/3_Hierarchical TDM.pdf, 10, 12, 14

PDH multiplexing solutions

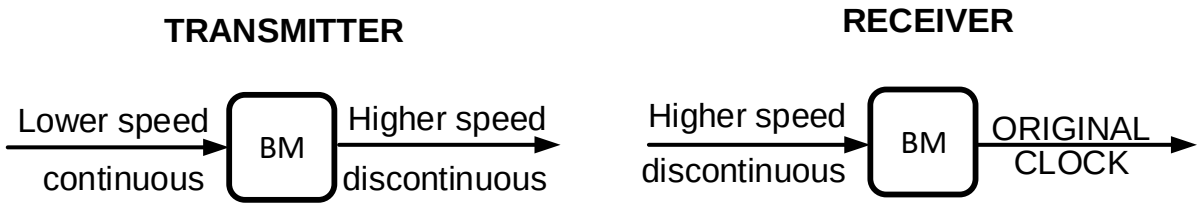
- Better solution – equalize the clock for all tributaries so that the bit rates are the same
  - Use faster clock rate than any of the tributaries
  - From time to time on each tributary a bit is doubled
  - Requires signaling for doubled bits (so that the receiver ignores them)

$f_{TRIBUTARY\ CLOCK} < f_{SEC.\ MUX\ CLOCK}$

Principle of positive justification – Transmitter



Principle of positive justification – Receiver



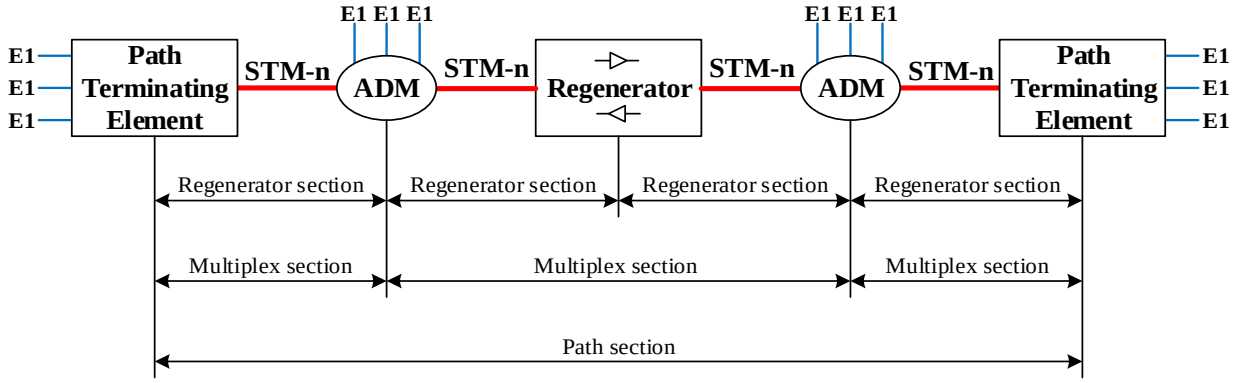
BM – buffer memory

3. SDH – architecture, sections and main network elements.

https://intranet.etc.upt.ro/~DIG_INT_NET/course/2015_2016/3_Hierarchical TDM.pdf, 34, 35

SDH architecture

- 3 layers SDH (SONET) – each layer introduces overhead in STM (STS) frames
  - Path section (Path)
  - Multiplex section (Line)
  - Regenerator section (Section)



STM-1 network elements

- PTE (Path Terminating Element)
  - end point device where the lower speed tributaries enter/leave the SDH Network
  - "Path Level" device
- ADM (Add/Drop Multiplexer)
  - extract and insert low speed tributaries into an STM stream
- Regenerator
  - digital signal regeneration
  - has dedicated overhead in the STM stream
- DCS (Digital CroSs connect) – not shown in diagram
  - cross-connect at the STM level down to individual E1 streams
  - an E1 stream from one STM trunk could be cross-connected to another STM trunk

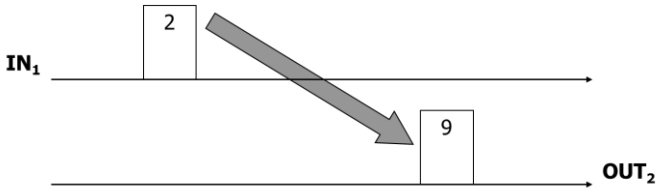
4. Digital switching – definition, the principle of the temporal switch, the principle of the spatial switch

https://intranet.etc.upt.ro/~DIG_INT_NET/course/2015_2016/4_Digital_switching.pdf, 1, 3, 8-10

Digital switch

DIGITAL SWITCH

- **any** TS of **any** INPUT (data flow) to **any** TS of **any** OUTPUT (data flow)



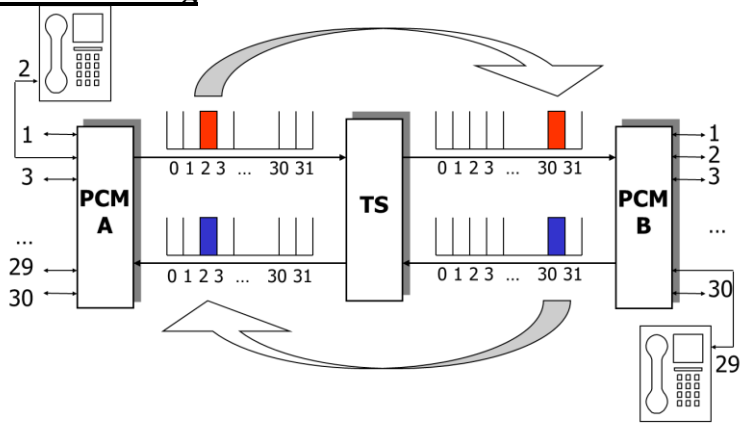
TEMPORAL SWITCH

- **any** TS of **any** data flow to **any** TS of the **same** data flow

SPATIAL SWITCH

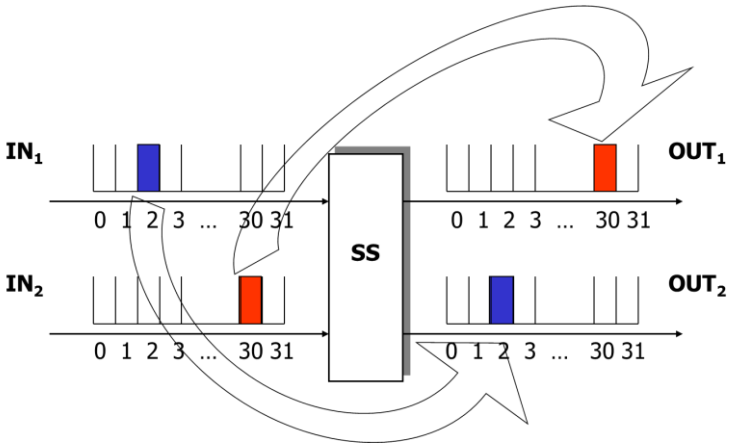
- **any** TS of **any** data flow to the **same** TS of **any** data flow

Principle of temporal switching



any TS of **any** data flow to **any** TS of the **same** data flow

Principle of spatial switching



any TS of **any** data flow to the **same** TS of **any** data flow

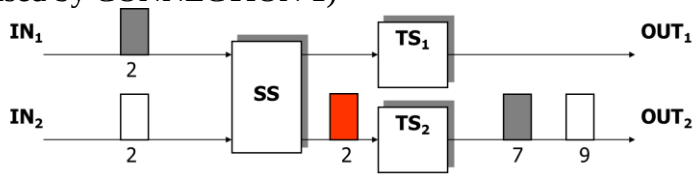
5. Digital switch blocking – definition and example of one switch with blocking and one switch without blocking

https://intranet.etc.upt.ro/~DIG_INT_NET/course/2015_2016/4_Digital_switching.pdf, 11-16

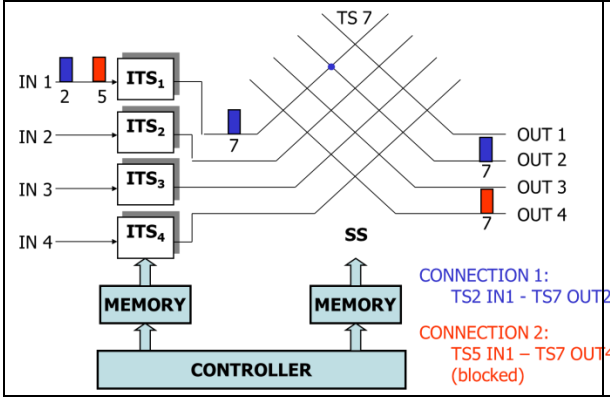
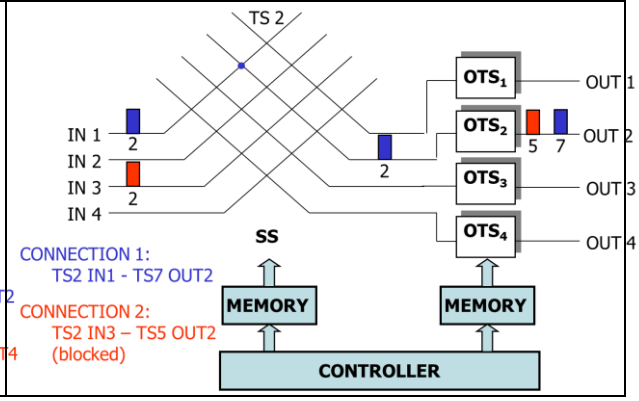
Blocking possibility in digital switch

A connection between 2 users is blocked by other already existing connection/s

CONNECTION 1: TS2 IN1 - TS7 OUT2
CONNECTION 2: TS2 IN2 - TS9 OUT2 – **blocked** (TS2 at OUT2 of SS is already used by CONNECTION 1)

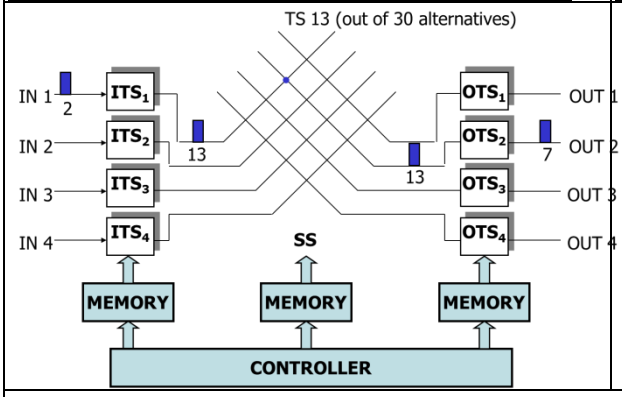


Examples of switches with blocking

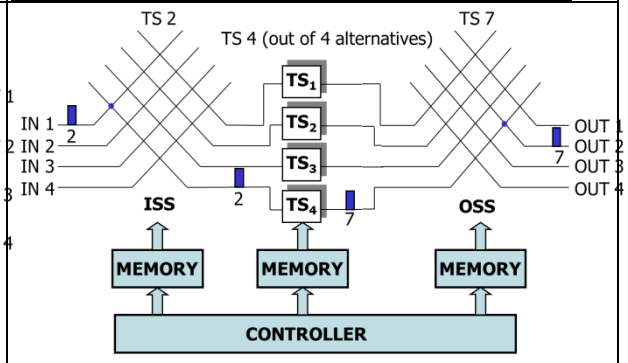
TS switch – 4 IN, 4 OUT – 120 channels	ST switch – 4 IN, 4 OUT – 120 channels
	

Examples of switches without blocking (new connections are no longer blocked by the already existing connections – alternative routes are available)

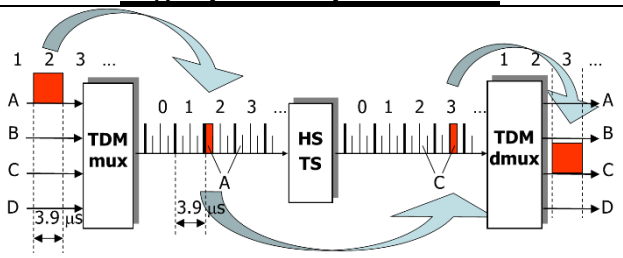
TST switch – 4 IN, 4 OUT – 120 channels



STS switch – 4 IN, 4 OUT – 120 channels



High speed temporal switch



4 x 2.048 Mb/s = 8.192 Mb/s

6. Enumerate and explain the ISDN conditions

https://intranet.etc.upt.ro/~DIG_INT_NET/course/2015_2016/5_ISDN.pdf, 1, 9, 10, 11

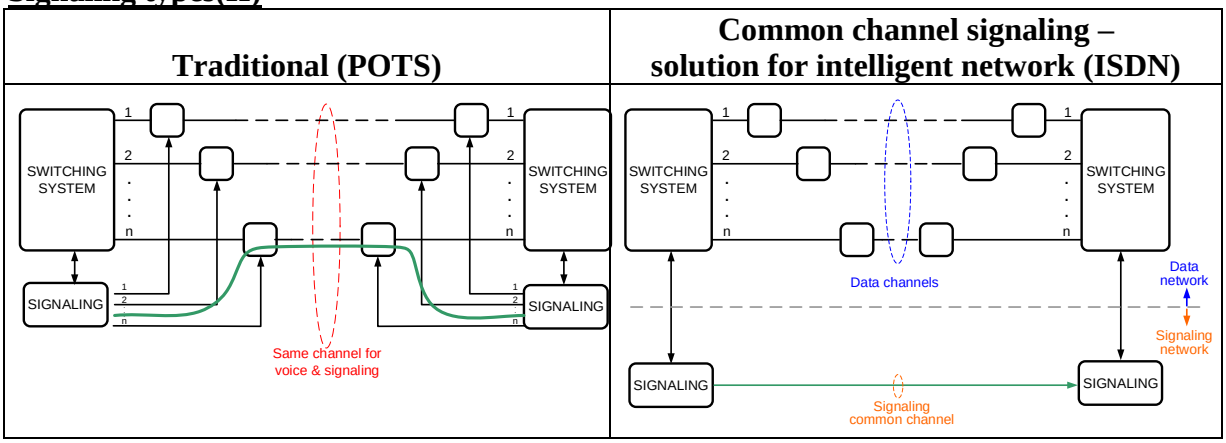
I.S.D.N. – Integrated Services Digital Network
CONDITIONS

1. Digital connections from **terminal to terminal**
   - digital signal
   - digital subscriber line - DSL
   - digital transmission
   - digital switching

2. Common-channel signaling – separate signaling network from the data network

3. Multiple network **access** for a wide range of voice and non-voice applications through the same interface

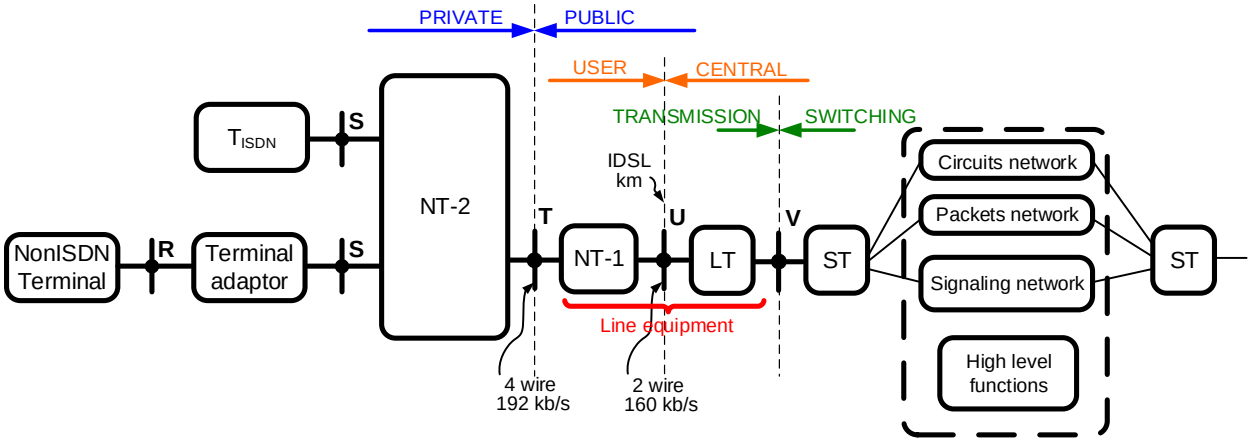
Signaling types(II)



7. ISDN function groups and reference points – definitions, significances and domain limits.

https://intranet.etc.upt.ro/~DIG_INT_NET/course/2015_2016/5_ISDN.pdf, 14,15,16

Function groups and reference points



LT (Line Termination) and **ST** (Switching Termination) – the physical and logical boundary between the digital local loop and the carrier's switching office

NT1(NetworkTermination1) – Customer Premises Equipment that performs the physical interface conversion between the dissimilar customer (4 wires) and network(2 wires)sides of the interface

NT2 (NetworkTermination2) – Customer Premises Equipment that performs the logical interface functions of switching and local-device control (local signaling)

TA(Terminal Adapter) – an interface-conversion device that allows communicating devices that don't conform to ISDN standards to communicate over the ISDN

The reference points:

- **R** – interfaces analog equipment to the ISDN
- **S** – equipment interface to the ISDN (4 wires, pseudo-ternary code, 192 kb/s bit rate)

- **T** – defined when interfacing a complex device to the ISDN (144 kb/s bit rate for BRI, 1984 kb/s in Europe and 1536 kb/s in the USA for PRI)
- **U** – interface between the NT1 and the LT (2 wires, 2B1Q coding, requires echo cancellation on the LT)
- **V** – of theoretical interest, separates transmission from switching, is relevant only in local exchanges

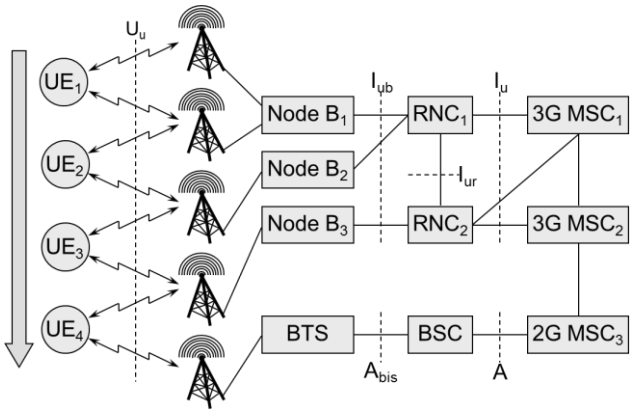
8. Handover types in 3G networks.

https://intranet.etc.upt.ro/~DIG_INT_NET/course/2015_2016/6_Mobile networks.pdf, 46, 50, 51

Handover

- Transfer of a link between 2 neighboring cells/antennas
- UMTS main handover classes:
  - Hard handover
    - Similar to GSM handover
    - Includes
      - Inter-frequency handover (change carrier frequency)
      - Inter-system handover (between UMTS and other systems)
  - Soft handover (new in UMTS)
    - Only available with FDD
    - Uses **macrodiversity**
      - fundamental characteristic of CDMA systems
      - mobile equipment communicates with up to 3 antennas simultaneously

Handover types in 3G



- **Intra-nod B, intra-RNC (softer handover)**

es between 2 different antennas of the same Node B (Node B_1)

- Node B_1 combines and splits the data streams

- **Inter-nod B, intra-RNC (soft handover)**

- UE_2 moves from Node B_1 to Node B_2
- RNC_1 supports the soft handover combining and splitting the data streams

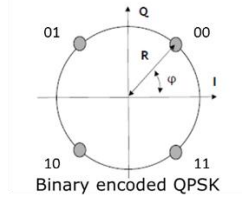
- **Inter-RNC**
  - UE_3 moves from Node B_2 toward Node B_3=> 2 possible situations
    - Internal (**soft**) inter-RNC handover, with RNC_1 acting as SRNC and RNC_2 acting as DRNC
    - External (**hard**) inter-RNC handover with relocation of the I_u interface
- **Inter-MSC**
  - MSC_2 takes over the connection and realizes a **hard** handover
- **Inter-system (hard handover)**
  - UE_4 moves from the 3G network to a 2G network
  - Important for areas with no 3G coverage

9. Digital modulation techniques used in LTE – list, characteristics and comparison.

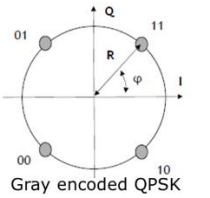
https://intranet.etc.upt.ro/~DIG_INT_NET/course/2015_2016/7_LTE.pdf, 22, 26

Digital modulations in LTE

- QPSK
  - Robust, less efficient
- QAM
  - High efficiency, less robust
- Gray encoding
  - neighboring symbols in constellation
  - only 1 bit different
  - limits the number of bit errors



Binary encoded QPSK



Gray encoded QPSK

LTE modulation summary

Modulation	No. of symbols	Bits/ symbol	Bit rate/ Baud rate	Robustness	No. of amplitudes	No. of phases
QPSK (4QAM)	4	2	2/1	+	1	4
16QAM	16	4	4/1	+/–	3	12
64QAM	64	6	6/1	–	9	52

10. OFDMA – principle of sub-carrier orthogonality, application in LTE.

https://intranet.etc.upt.ro/~DIG_INT_NET/course/2015_2016/7_LTE.pdf, 30, 35, 38

LTE multiple access

- OFDMA (Orthogonal Frequency Division Multiple Access)
  - Multiple equally spaced orthogonal subcarriers
  - Data stream is split in multiple sub-streams
    - Each sub-stream modulates a subcarrier using 64QAM, 16 QAM or QPSK
  - used on DL
- SC-FDMA (Single Carrier Frequency Division Multiple Access)

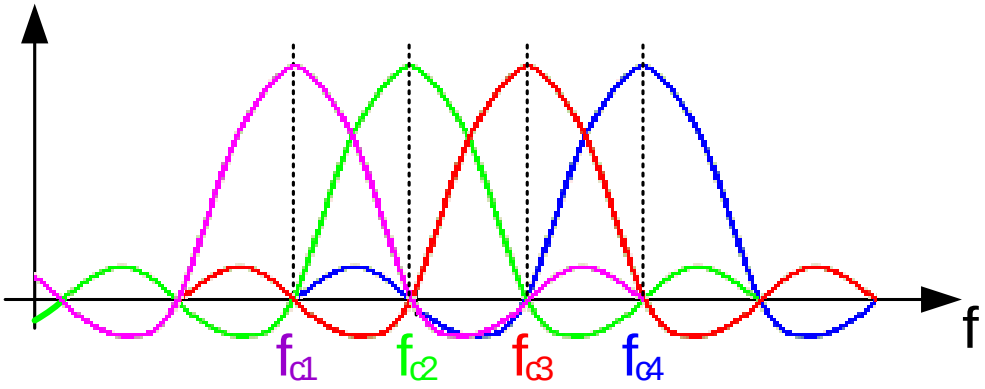
- Uses only a reduced number of sub-carriers (contiguous group)
- lower PAPR (Peak to Average Power Ratio) compared to OFDMA
- used on UL
- Inappropriate for DL
    - eNB uses all available sub-carriers
    - eNB transmits to multiple UEs at the same time

OFDMA

- Data stream is split into multiple sub-streams
- Frequency bandwidth divided into multiple sub-bands (sub-carriers)
- Each data sub-stream modulates (QPSK, 16QAM or 64QAM) a sub-carrier
- Sub-carrier orthogonality
    - the signal sent on a carrier does not interfere with signals sent on other carriers
    - achieved by proper choice of sub-carrier spacing
        - $\Delta f = 1/T$ (T – OFDMA symbol period)
        - in LTE, **T = 66.7 µs** => **Δf = 15 kHz**

Orthogonal carriers

- OFDM spectrum example:
    - 4 carriers spaced by $\Delta f = 1/T$ (= 15 kHz for LTE)
    - at each carrier frequency (e.g. f_{c2})
        - there is a maximum of the spectrum of the signal transmitted on that carrier (f_{c2})
        - all spectra of signals transmitted on other subcarriers (f_{c1}, f_{c3} and f_{c4}) are crossing 0 => => orthogonality (no interference)



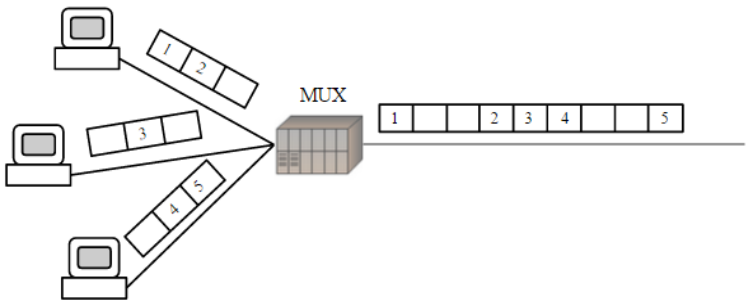
DATA COMMUNICATIONS – S20

1. Multiplexing. Definition. Types description: synchronous TDM, statistical (asynchronous) TDM, FDM,wavelength multiplexing. Explain, using a scheme the TDM, FDM.

Multiplexing is a method by which multiple data streams, coming from different sources, are combined and transmitted over a single communication channel. The device that combines multiple data streams into one is called multiplexer (MUX). The reverse process, called demultiplexing, extracts the original data streams at the destination. This task is realized by a device called demultiplexer (DMUX).
Some methods used for multiplexing data are:

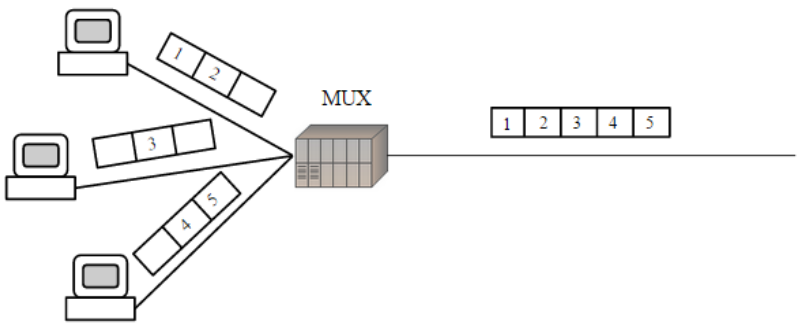
- Synchronous time-division multiplexing (STDM)
- Asynchronous time-division multiplexing (ATDM)- called also statistical multiplexing
- Frequency-division multiplexing (FDM)
- Wavelength multiplexing

In synchronous TDM, shown in figure below, there is a static allocation for each source, the same interval of time, in the same order. Time slots are allocated to sources, whether they have or not information to transmit. In this way, the channel capacity might be wasted.



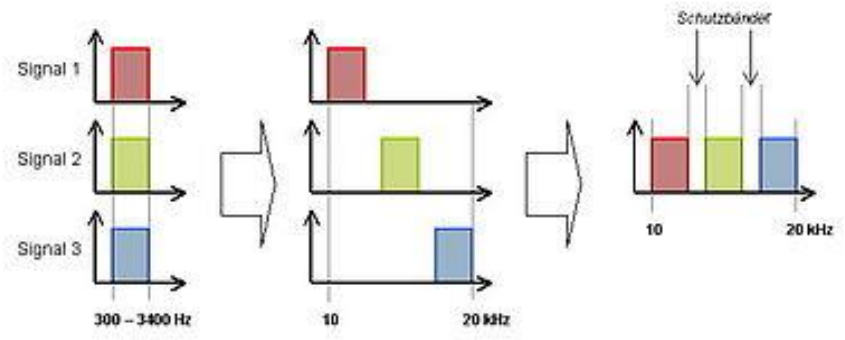
Synchronous time-division (STDM)

An efficient alternative of the synchronous TDM is the *Statistical TDM*, also called *Asynchronous TDM (ATDM).* In ATDM is allocated bandwidth to a variable number of users as needed, in a dynamical manner as shown in figure below. In this case the transmitted packets may not arrive in order and the demultiplexer cannot simply identify the source based on data packets reception. For this the sequence order and the explicit address of source must be specified.



Static TDM is carried out at the physical layer in the OSI model and TCP/IP model. Statistical multiplexing is carried out at the data link layer and above.

In *Frequency Division Multiplexing (FDM),* the available bandwidth of a single physical medium is subdivided into several independent frequency channels. FDM assigns "frequency ranges" to each user on a medium, all signals being transmitted at the same time, each one using a different frequency. The most common examples of FDM are the radio/TV broadcasting, where multiple radio signals at different frequencies pass through the air simultaneously, or the cable television, where many TV channels are carried on a single cable, at the same time.

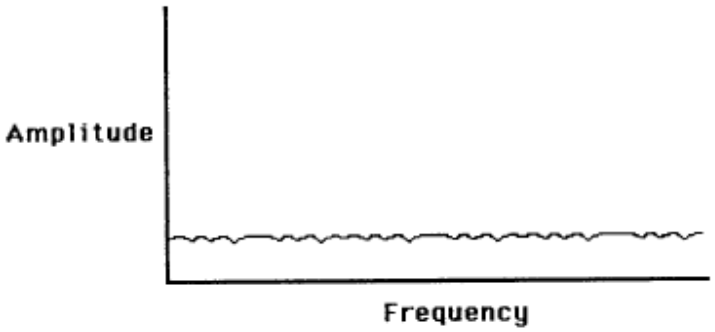


Wavelength division multiplexing (WDM) is a particular case of FDM used in optical fiber communications. The inputs and outputs of WDM are different wavelengths of light (colors).

2. What is thermal noise? Give the expression of the power spectral density of a thermal noise, indicating the meaning of each parameter and the measurement units.

Thermal noise is generated by the thermal agitation of electrons.

- Uniformly distributed in frequency, generally modelled as white noise
- Cannot be eliminated
- Present in all electronic devices and transmission media
- Function of temperature
- Particularly significant for satellite communications



Thermal noise is characterized by a near uniform distribution of energy over the frequency spectrum

The amount of thermal noise in the band of 1Hz is $N_0=kT$.
Where:

- N_0 is the noise power spectral density [Watts/Hz] –independent of frequency
- k-is Boltzmann constant=1,38 $.10^{-23}$ J/°K
- T –is temperature in Kelvins degrees (absolute)

The amount of thermal noise in a bandwidth of B Hz is dependent on frequency:

$$N = kTB$$

Notice that, larger the bandwidth, larger will be the amount of thermal noise "seen" by the receiver. We may therefore say that larger bandwidth transmissions are more affected by the thermal noise, compared to the narrower bandwidth transmissions.
dBW

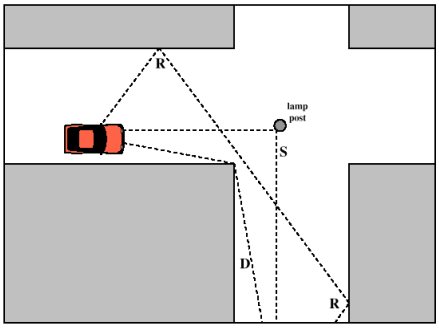
$$N = 10\log k + 10\log T + 10\log B =$$
$$-228{,}6 + 10\log T + 10\log B$$

3 What is multipath? Which are its causes and its effects on signal transmission?.

Multipath appears in:

- in terrestrial, fixed microwave
- in mobile communications

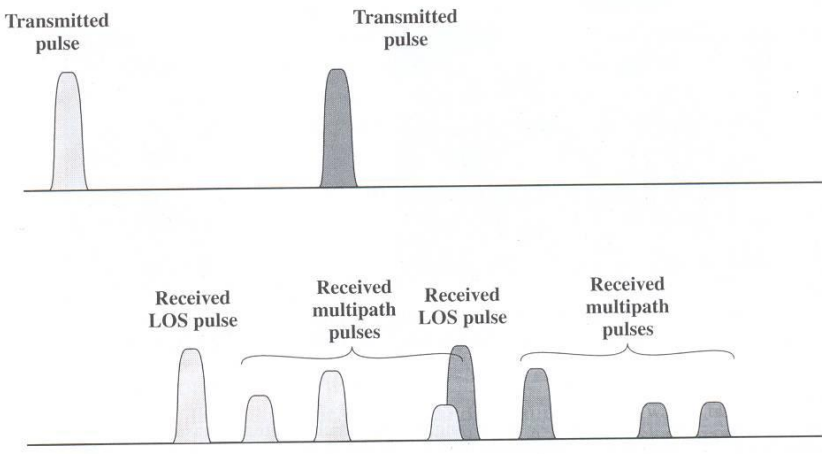
Due to the existent obstacles the signal can be reflected, diffracted, scattered so that multiple copies of the same signal, with varying delays and attenuation might be received. In extreme cases, the receiver may capture only the reflected signal and not the direct one
There are three important propagation mechanisms which can be seen in figure below.
R Reflection when a signal encounters a surface large relative to its wavelength (a ground refelectide wave for mobile communications)
D Difraction at the edge of impenetrable objects, large compared to signal wavelength
S Scattering when a signal encounters a surface of size on the same order of magnitude as its wavelength or less.



Effects of multipath:

- Multiple copies of a signal may arrive at different phases.If phases add destructively, the signal level relative to noise declines, making detection more difficult
- Intersymbol interference (ISI) One or more delayed copies of a pulse may arrive at the same time as the primary pulse for a subsequent bit as shown in figure below.

Solution-Reinforcement and/or cancellation of the multipath signals. The OFDM technique was especially designed to deal with the multipath problem.



4. Write down the formula describing the Shannon capacity theorem for noisy channels, explain the meaning of each parameter and interpret the relation.

The Shannon capacity theorem widely used form is:

$$C = B\log_2\left(1+\frac{S}{N}\right)$$

Where

- C is the channel capacity, the rate at which data can be transmitted over a given communication path, under given conditions

- S/N is signal to noise ratio of power expressed in absolute value, not expressed in dB!

Shannon's formula expresses the theoretical maximum rate that can be achieved referred to as the error free capacity. In practice much lower rates are achieved. One reason is that only white noise is considered (not impulse noise, nor attenuation)

Shannon proved that if the actual information rate on a channel is less than the error-free capacity, then it is theoretically possible to use a suitable signal code to achieve error-free transmission through the channel. Currently the Shannon capacity cannot be achieved even in an ideal white noise condition of transmission, due to encoding issues, such as coding length and complexity environment.

For a given level of noise the channel capacity can be increased either by increasing S or B. But increasing signal may increase the nonlinearities in the system and and this may determine an increase in intermodulation noise. Also notice that increasing B means that thermal noise will be increases too and this decreases the S/N ratio.

5. What is data rate? What is modulation rate? Explain what means an efficient transmission giving an example. Compare a NRI encoding with a Manchester encoding.

Data rate is the rate at which data is transmitted and it is expressed in bits per sec.

$$R = \frac{1}{T_b}$$

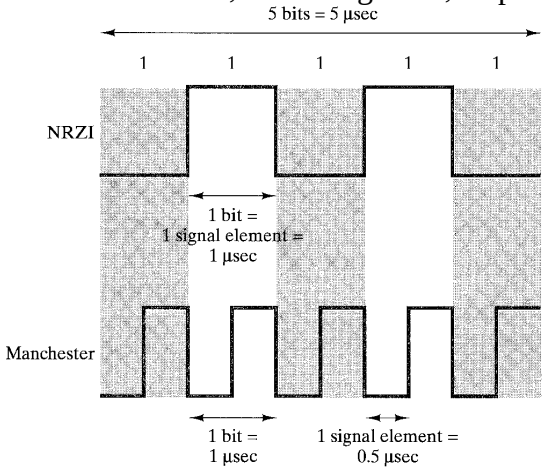
T_b being the bit duration (time taken to emit one bit)
While data rate shows how many bits can be sent on a second, the modulation rate is related to the physical signal transmitted through the medium.
Modulation rate is the rate at which the signal level is changed. It is measured in Baud, number of signal elements per second. Relation between modulation rate and data rate is:

$$D = \frac{R}{N} = \frac{R}{\log_2 M}$$

Where:

- D = modulation rate [Baud]
- R = data rate [bps]
- N =number of bits per signal element

The modulation rate can be lower or higher than the data rate. A good efficiency of transmission is achieved if data rate is higher comparative to modulation rate (R≥D). But this requires more complex modulation schemes, with a higher N, respectively M.

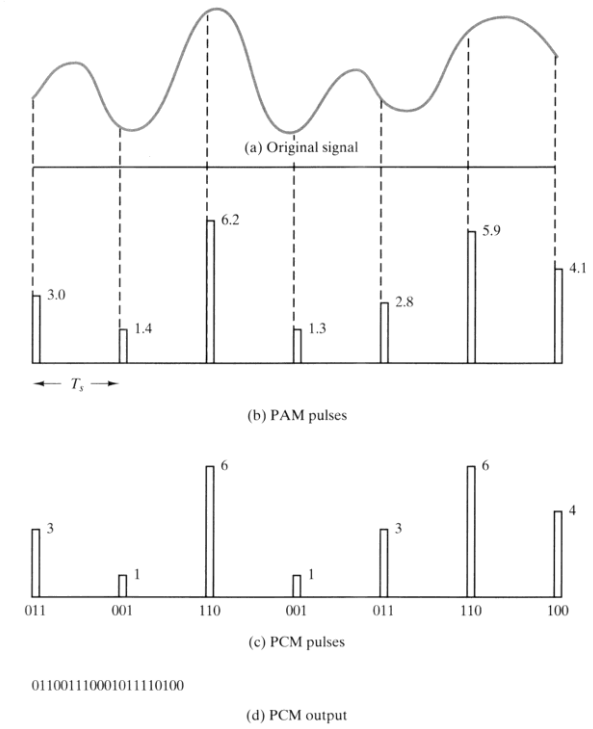


Two examples can be seen in figure above.

- In case of a NRZ code during one bit representation, the signal stays on a constant voltage level (e.g. +1V or -1V) consequently D=R.
- In case of Manchester code during one bit representation, the signal can stays half of the bit period on a certain voltage level (e.g. +1V) and the other half on the opposite level (-1V). The modulation rate is twice the data rate D=2R consequently a reduced efficiency comparative to NRZ is achieved.

6. What is Pulse Code Modulation? Which is the error introduced in PCM and which are the ways of reducing it?

PCM is an analog to digital signal digitizing technique, based on the sampling theorem which states:
If a signal x(t) is sampled at regular intervals of time and at a rate higher than ! twice the highest significant signal frequency, then the samples contain all the information of the original signal. The function x(t) may be reconstructed from these samples by the use of a low-pass filter.
Ex for voice data considering B=4kHz a data rate of R=8kbps is sufficient to characterize the voice signal.
See the following PCM example:



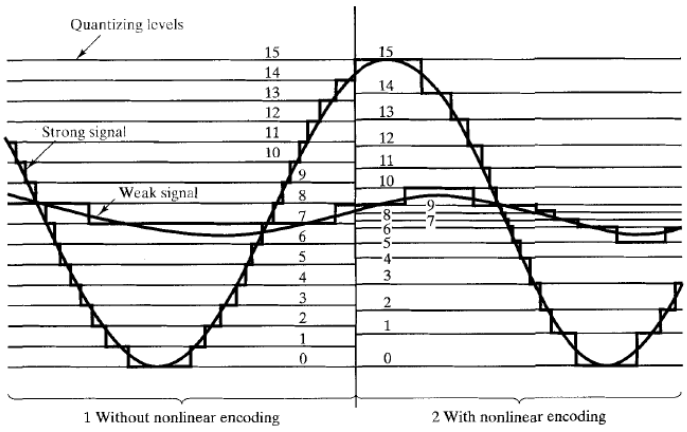
- **Original signal**
  has continuous amplitudes in its dynamic range
- **PAM - signal** is a discrete constant period, pulse train having continuous amplitude values
- **Quantized PAM** signal has only the values that can be quantized by the words available (here by 3 bit words)

To each analog PAM sample is assigned a binary code. The digital signal consists of a block of *n* bits, where each *n*-bit number is the amplitude of a PCM pulse.

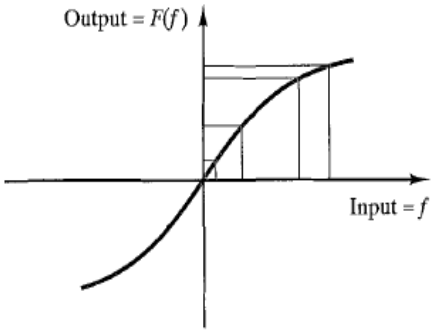
With a code having 2^n bits there will be obtained n quantization levels, as examples:

2 bits – 4 quantization levels
3 bits – 8 quantization levels
4 bits -16 quantization levels

Quantization error/noise is unavoidable, consequently regenerated analog data cannot be 100% the same as original.
To reduce quantization error: we have to increase the quantization number of levels, to 64 quantization levels (6 bits), and/or to increase the sampling rate (to decrease sampling time interval).
The problem with equal spacing (the same step of quantization –uniform quantization) is that the mean absolute error for each sample is the same, regardless of the signal level. Consequently, lower amplitude values are relatively more distorted. By using a greater number of quantizing steps for signals of low amplitude, and a smaller number of quantizing steps for signals of large amplitude, an important reduction in the overall signal distortion is achieved (see the following figure)

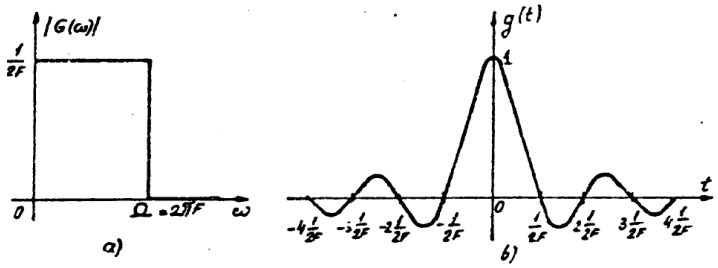


The same effect can be achieved by using uniform quantizing but companding (compressing-expanding) the input analogue signal. Companding is a process that compresses the intensity range of a signal by amplifying more weak signals than strong signals. At output, the reversed operation is performed. Nonlinear encoding can significantly improve the PCM S/N ratio Ex: For voice signals, improvements of 24 to 30 dB have been achieved. A typical companding function is shown in figure below:



7. The ideal low pass filter and Nyquist criterion for zero ISI. Drawbacks of using the ideal low pass filter.

The transfer function and the impulse response of the ideal low-pass filter are the followings:



The ideal low-pass (called also brick wall) filter has a cut-off frequency F=1/T. The impulse response waveform crosses zero every T/2 seconds. If a symbol is issued every T/2 seconds, transmission can be made without ISI, satisfying the Nyquist criteria for zero ISI.

$$g_k = \begin{cases} 1, \text{if } k = n \\ 0, \quad \text{otherwise} \end{cases}$$

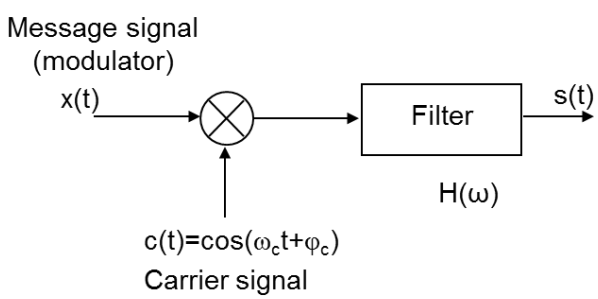
The modulation rate in this case is the Nyquist ideal modulation rate, 2F symbols/s. But ideal filter is practically impossible to be generated.

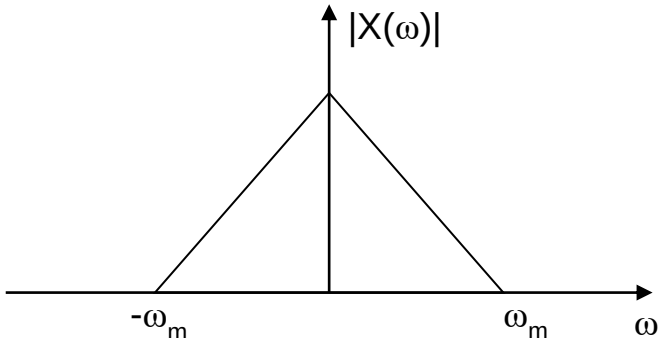
Drawbacks of using sinc pulse shaping filter:

- A sinc waveform is of infinite length, having tails of energy which extend to infinity. One can only design a finite duration waveform, which is an approximation of the real sinc pulse. Its time-domain "windowing" leads to a spectrum which is not an ideal low-pass function any more. Consequently, truncating the sinc waveform will increase its sensitivity towards the ISI phenomenon.

- The side-lobes of the cardinal sine are still important (even if they have a significantly lower energy compared to the main lobe. Actually, the pulse tails that fall in the adjacent symbol times, decay at the rate of 1/t. Consequently, if some timing error occurs (e.g. a receiver synchronization error), signals corresponding to adjacent symbols will significantly affect the value of the sample corresponding to the current symbol, thus creating ISI. Higher data rate (reduced T_s) needs larger bandwidth. The signal will be more sensitive to channel properties, since each channel has a limited bandwidth.

8. Consider the simplest case of product amplitude modulation from the figure. Explain the following terms: DSB-AM, SSB-AM. Select the inferior and superior SB by using a bandpass filter H(ω) and draw the correspondent spectrum.





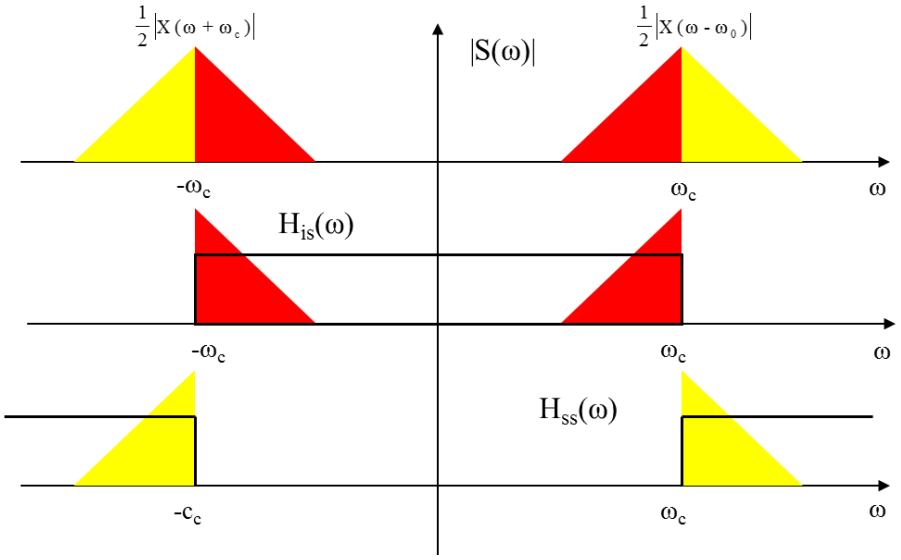
DSB-AM comes from double side band amplitude modulation. SSB-AM comes from single side band amplitude modulation.

As a result of the modulation, the spectrum of the message signal shifts from "0" to carrier frequency ω_c. The signal transmitted through the channel has a spectrum located to the carrier frequency. The filter H selects the desired band.

The spectrum of the modulated signal passed through a filter with H(ω) transfer function is:

$$S(\omega) = H(\omega)\left[\left[\frac{1}{2}X(\omega_c + \omega) + \frac{1}{2}X(\omega - \omega_c)\right]\right]$$

The filter H selects the lower (inferior) or the upper (superior) side-band of a DSB AM signal, leading to Single Side Band (SSB) AM



9. What is phase modulation and PSK? Explain the meaning of terms PSK, BPSK and QPSK. Give the analytical expression of a general PSK signal and particularize in the case of a BPSK and QPSK signal. Graphically represent a BSK signal.

Phase Modulation is a method used to transmit analog or digital signals, in which the information is carried by the initial phase of a high-frequency carrier. When the modulator is digital, the phase modulation is referred to as phase shift keying (PSK).

BSK comes from binary shift keying and refers to the fact that the phase modulated signal has two phases. QPSK comes from quadrature phase shift keying.

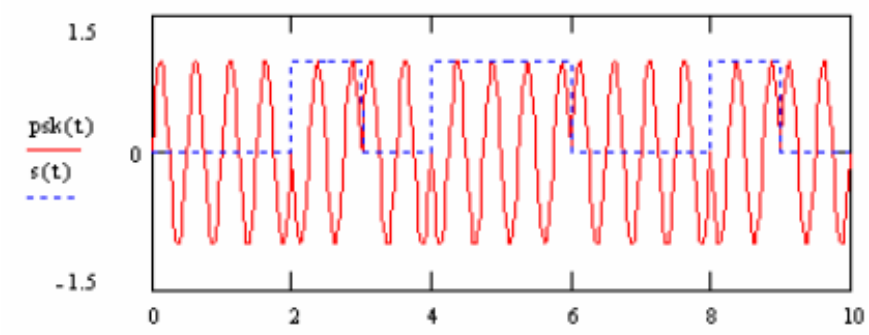
General analitical expession of PSK is:

$$s(t) = U_0 \cos[\omega_0 t + k_P x(t) + \theta]$$

Where k_P is phase sensitivity factor, peak phase deviation over one symbol.

For the BPSK case, the modulation is implemented by simply inversing the sign ($0^o/180^o$ phase shift) s(t) is the modulator and psk(t) is the modulated signal

$$PSK(t) = \begin{cases} \sin(2\pi f t) & for\ bit\ 1 \\ \sin(2\pi f t + \pi) & for\ bit\ 0 \end{cases}$$



Two types of binary phase modulation are used, known as "A law " respectively " B law “ which have the the following truth tables

A	φ_A
0	180°
1	0

B	φ_B
0	-90°
1	90°

10. Write down the expression that describes the orthogonality of the OFDM carriers. What is the relation between the OFDM symbol duration (T) and the fundamental frequency (f_0)?

The OFDM carriers are orthogonal if their frequencies are f_0, $2f_0$, $3f_0$ etc, because the integral of the product of two sinusoids (cosinusoides) is zero. In general for all integers n and m, sin nx, sin mx, cosnx, cosmx are all orthogonal to each other.

$$\frac{2}{T}\int_{kT}^{(k+1)T} \sin(mf_0t)\cdot\sin(nf_0t)\cdot dt = \begin{cases} 1, \text{ if } m = n \\ 0, \text{ if } m \neq n \end{cases} \quad (1)$$

This means that there is no interference between the carriers

In practice there are used for carriers complex exponentials of limited duration (using a window function). Their duration equals OFDM's symbol time (T).

The orthogonality is achieved if: $f_0=1/T$

1. *Digitization parameters and data rates for voice and hi-fi audio*

https://intranet.etc.upt.ro/~AVS/Course/1_MULTIMEDIA.PDF, 15,16

- **High-quality stereo standard**
  - CD standard, hi-fi music, 20 kHz audio bandwidth
  - 2 channels
    - for **stereo** recording and transmission
  - f_E = 44.1 kHz
    - **sampling rate**, according to Shannon's theorem
  - n = 16 bits
    - for **quantization** with SNR = 96 dB

  ⇨ data rate: 2 × 44.100 × 16 = 1 411 200 bits/s

- **Speech-quality standard**
  - telephony standard, voice, 3,4 kHz audio bandwidth
  - 1 channel
    - for voice **recognition**
  - f_E = 8 kHz
    - **sampling rate**, according to Shannon's theorem
  - n = 8 bits
    - for **quantization** with SNR = 48 dB

  ⇨ data rate: 1 × 8.000 × 8 = 64.000 bps

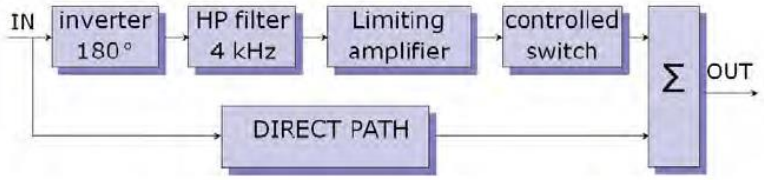
2. Noise reduction principles

https://intranet.etc.upt.ro/~AVS/Course/2_SOUND.PDF, 23-28

Playback noise reduction (I+II)

- **NOISE** ⇔ signal with low level and middle to high **frequency**

  ⇨ such a signal can be identified and **rejected** (noise gate)
- **Example**: Philips **DNL** (*Dynamic Noise Limiter*)



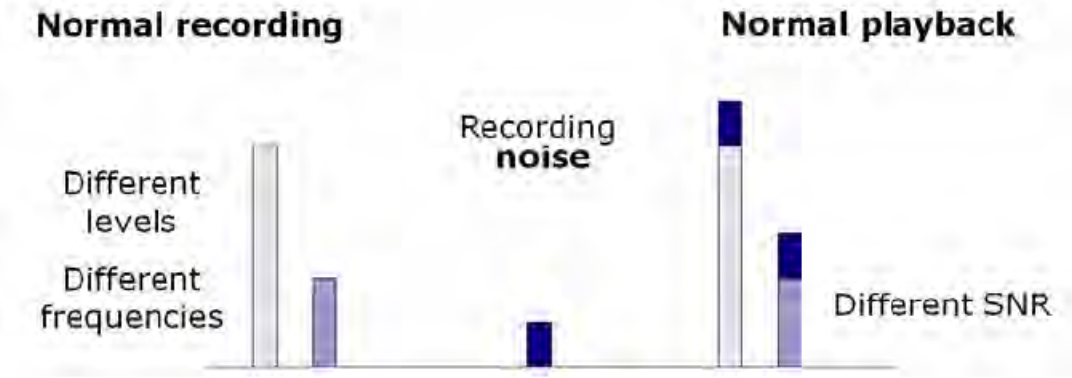
IN: signal with noise

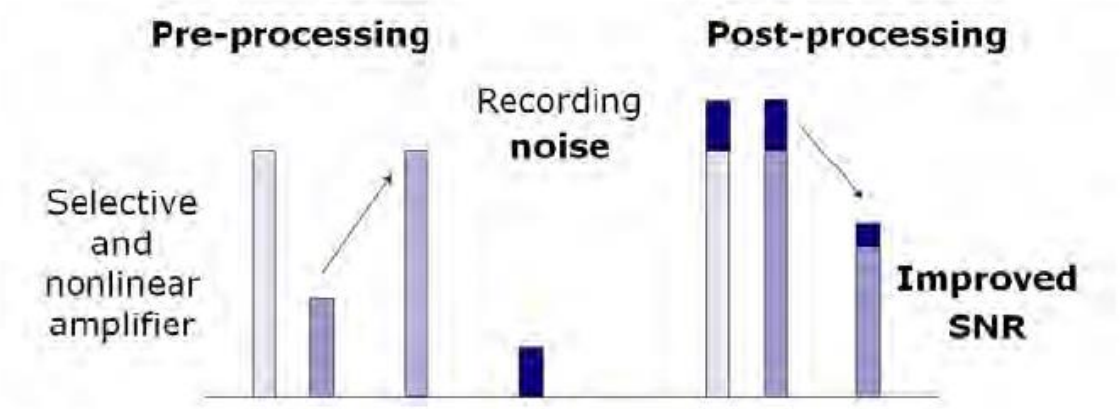
OUT: signal with **improved SNR** with **8 dB**

- **DNL advantage**:
  - works with any recording system on **any playback system**
- **How DNL works in different situations:**
  - during the **pause** between melodies
  - high level recorded music
  - low level recorded music
- **DNL disadvantage**:
  - it cannot make the difference between noise and the real signal

Recording & playback noise reduction systems (I+II)

- The systems perform:
  - signal processing before recording
  - opposite processing after playing back





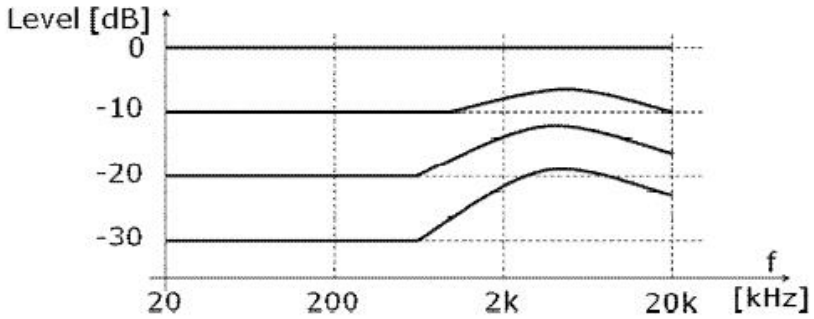
Advantage:

- the real signal is **not altered** and obtained with a **high SNR**

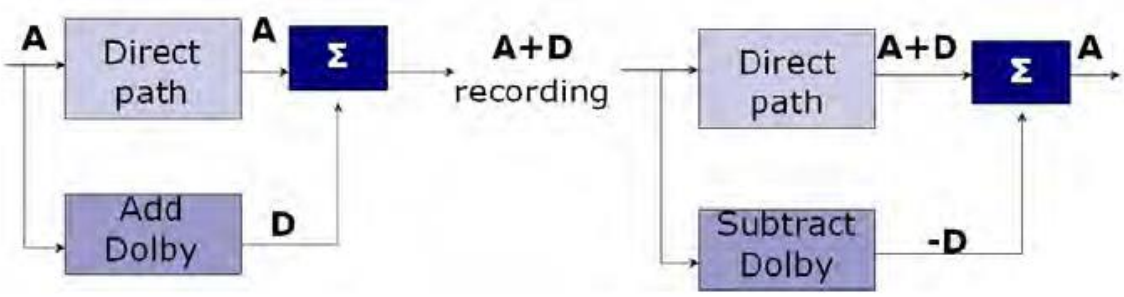
Disadvantage:

- it only works on the same system (record and playback)

Dolby system (I+II)



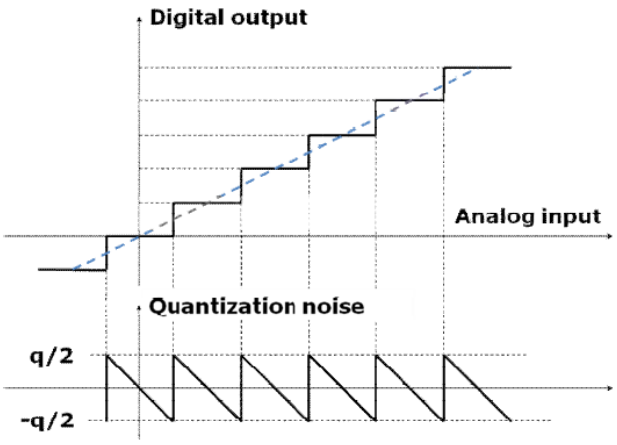
- **NOISE**:
  - high frequency (1 ÷ 15 kHz)
  - low level (-20 ÷ -40 dB)
- **DOLBY** circuits:
  - amplify **nonlinearly** and **selectively** when recording
  - performs opposite processing on playing the signal
  - **Increases SNR** with 9 dB

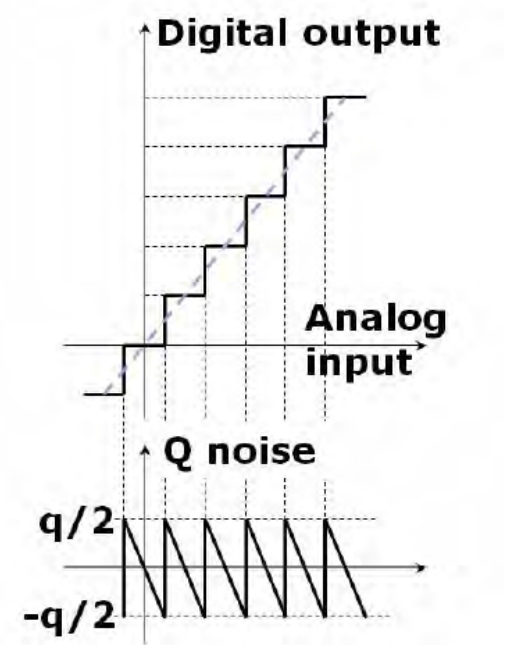


3. Quantization techniques

https://intranet.etc.upt.ro/~AVS/Course/2_SOUND.PDF, 36, 37, 41, 42

Uniform quantization (I+II)





- **decision levels** (analog input)
  - ☐ **uniform**
- **quantization levels** (digital output)
  - ☐ **uniform**
- **quantization steps** (q) are **constant:**
  - ☐ for low level signal
  - ☐ for high level signal
- **quantization noise** (error): -q/2 ÷ q/2

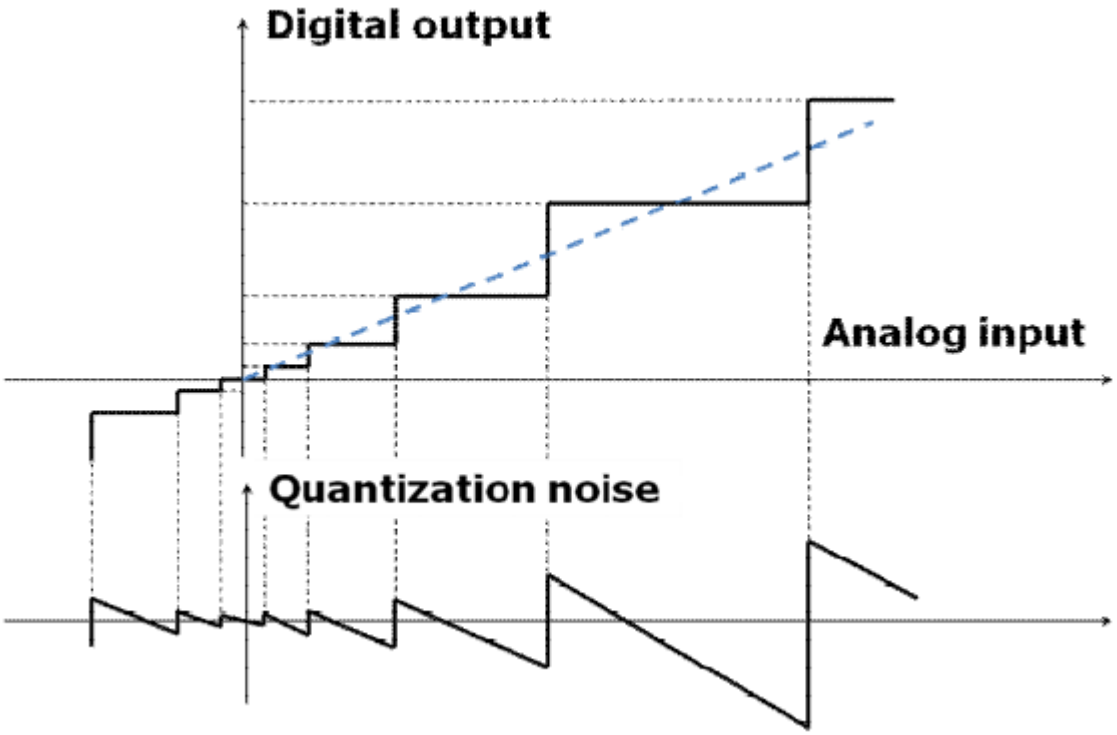
RESULT

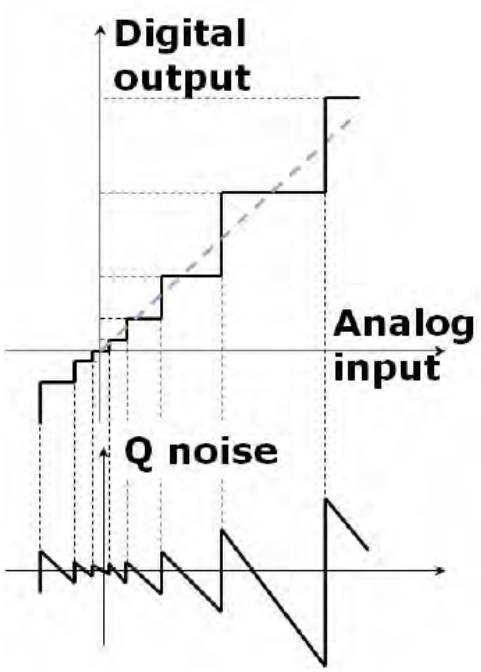
- **low level signal with** constant quantization error ⇨ **low SNR**
- **high level signal with** constant quantization error ⇨ **high SNR**

CONCLUSION

- **low general SNR (⇔ low quality)**

Non-uniform quantization (I+II)





- **decision levels** (analog input)
  - **non-uniform**
- **quantization levels** (digital output)
  - **non-uniform**
- **quantization steps** (q) are **different:**
  - for low level signal
  - for high level signal
- **quantization noise** (error):
  - **non-constant**

RESULT

- **low level signal with** low quantization error ⇨ **high SNR**
- **high level signal with** high quantization error ⇨ **high SNR**

CONCLUSION

- **high general SNR (⇔ high quality)**

4. The digital photo camera – adjustments, structure

https://intranet.etc.upt.ro/~AVS/Course/3_EC_image_web.pdf, 6-9

Photographic image acquisition (II)

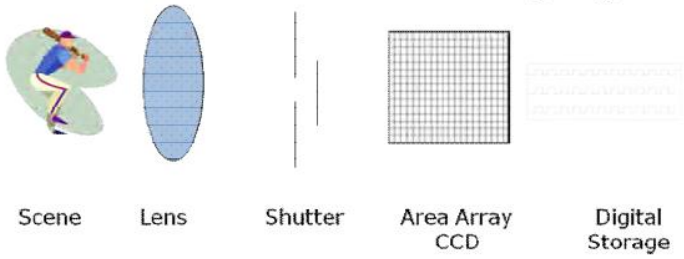
- **Conventional** image **capture** needs the following main components:
  - LENS
    - to **focus the light** from a scene onto a photosensitive film (silver)
  - IRIS
    - to control the **amount of light** which hits the film
  - SHUTTER
    - to control the **timing** of the light exposure of the film

Electronic image acquisition (I+II)

- The **electronic** image is obtained using:
  - traditional elements: lens, iris, shutter
  - additional components:
    - **CCD** (Charge Coupled Device)
      - image **scanning** and **photo-electric** conversion
    - **ADC** (Analog to Digital Converter)

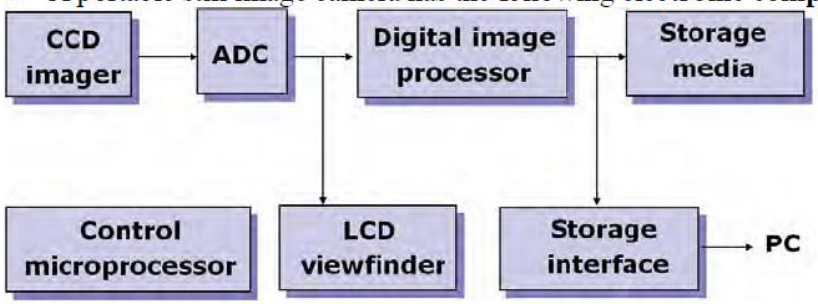
- delivering the **digital format** of the image

- **Digital storage media**
  - **electronic** memory, **magnetic** support (disk or tape), optical support



Digital photo camera (I)

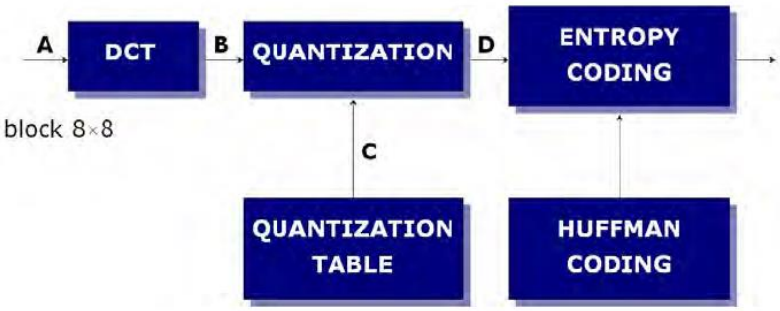
- A portable still image camera has the following **electronic components**:



5. The principle of JPEG compression

https://intranet.etc.upt.ro/~AVS/Course/3_EC_image_web.pdf, 62-66

JPEG Methodology (I+II+III)



- **DCT**
  - transforms **time** representation block **A** (lot of data points)

- in **frequency** representation block **B**
  (few data points – few frequency components)

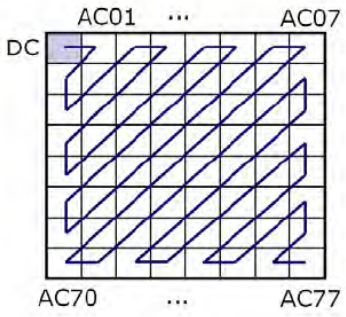
- **QUANTIZATION**
  - reduces **non-uniformly** the accuracy of coefficients, **D**, according to the quantization table **C** (**4 tables** implemented in JPEG algorithm):
    - **low frequency** with higher accuracy
      (small steps, non-zero values)
    - **high frequency** with lower accuracy
      (big steps, most values equal to zero)
- **ENTROPY CODING**
  - is used to obtain **data compression**
  - zig-zag scanning is used to obtain **long sequences of "zero"**
    - **RLE** (Run-Length Encoding) - offers an excellent compression
    - **Huffman coding -** is used to obtain higher compression factor

Discrete Cosine Transform (I+II)

- **DCT** (similar to Fourier transform) converts data from
- from **time domain**
  - 8×8 pixels block:
    - rows 0 ÷ 7
    - columns 0 ÷ 7
- to **frequency domain**
  - 8×8 coefficient matrix
  - 00 position
    - DC coefficient
      - average of the 8×8 block
  - 01 ÷ 77 positions
    - AC coefficients
      - low frequency in the upper left corner
      - high frequency elsewhere

Zig-zag sequencing

- starts with low frequency coefficients (non-zero),
- then high frequency coefficients (zero);
- results a long sequence of zeros, after a few significant values, easy entropy coding (RLE, Huffman)

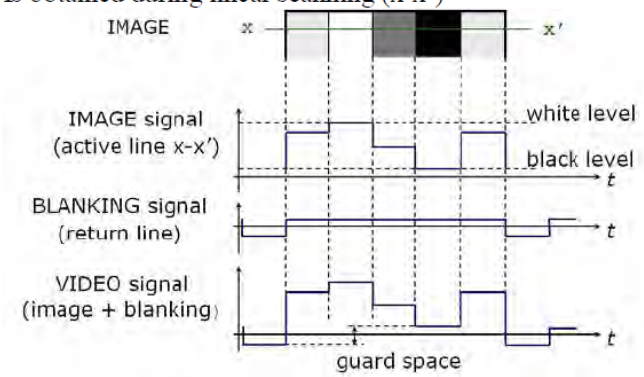


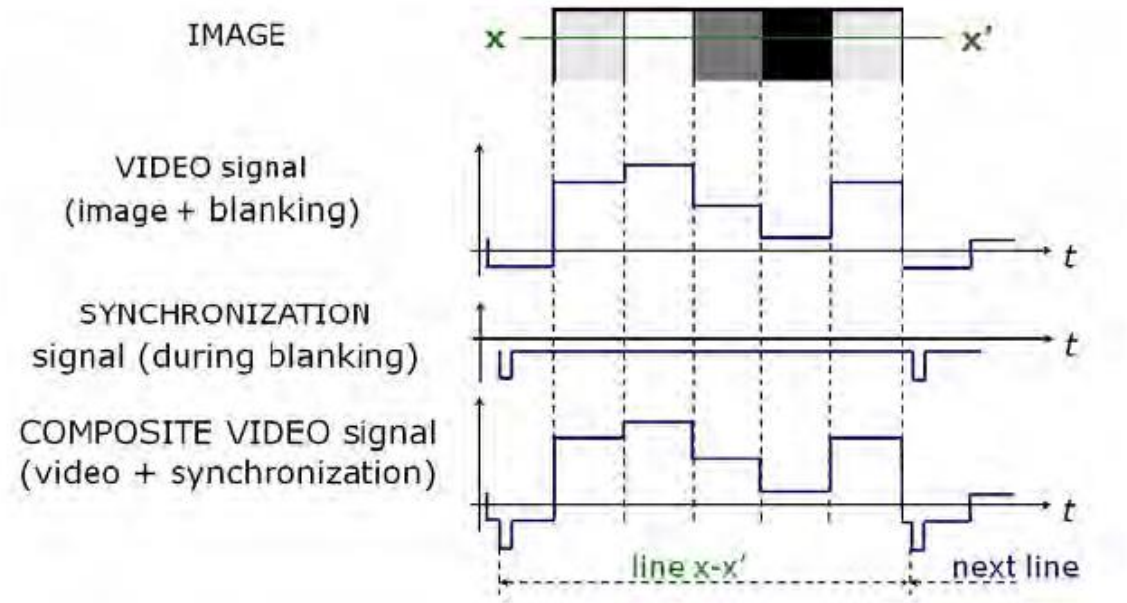
6. The composite video signal (components, parameters, TV line oscillogram)

https://intranet.etc.upt.ro/~AVS/Course/4.1_EC_TV_web.pdf, 9, 10, 12

Composite video signal (I+II)

Is obtained during linear scanning (x-x')





Frequency of composite video signal (II)

- Aspect ratio
  - 4 × 3
- Vertical resolution
  - 575 visible lines (out of 625)
- Horizontal resolution

  For best resolution perception, the pixel must be **square**
  - 4 / 3 × 575 = 766 pixels

7. Color TV signals

https://intranet.etc.upt.ro/~AVS/Course/4.1_EC_TV_web.pdf, 21-23

Color TV signals (I+II)

- Luminance of a (color) image is used in black-and-white television:

  Y = 0.3×R + 0.59×G + 0.11×B
- Using R, G, B signals would be incompatible with the old TV system.
- Compatible color TV systems use:
  - Y – **luminance**

    (for correct processing by black-and-white TV sets)
  - C – **chrominance**

    (color information only, no brightness information)

⇨ **color difference** signals: **R-Y, G-Y, B-Y**

- From the 4 signals, only 3 are used:
  - luminance
    - $Y = 0.3 \times R + 0.59 \times G + 0.11 \times B$
  - chrominance (2 color difference)
    - $R\text{-}Y = 0.7 \times R - 0.59 \times G - 0.11 \times B$
    - $B\text{-}Y = -0.3 \times R - 0.59 \times G + 0.89 \times B$

Compatible TV signals (I)

- **Luminance**

  $E_Y = 0.3 \times E_R + 0.59 \times E_G + 0.11 \times E_B = 0 \div 1$
- **Color difference**

  $E_{R-Y} = 0.7 \times E_R - 0.59 \times E_G - 0.11 \times E_B = -0.7 \div 0.7$

$$E_{G-Y} = -0.3 \times E_R + 0.41 \times E_G - 0.11 \times E_B = -0.41 \div 0.41 \text{ (not transmitted)}$$

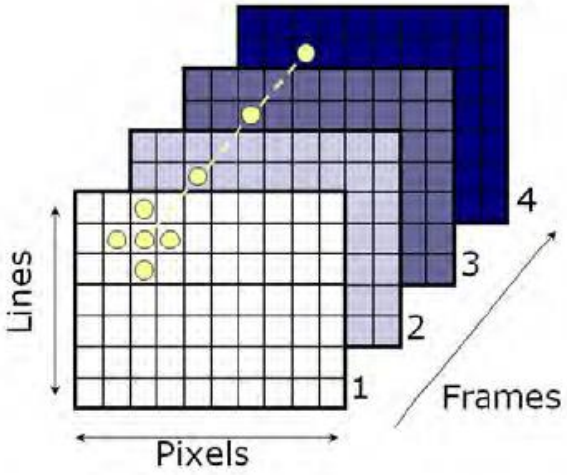
$$E_{B-Y} = -0.3 \times E_R - 0.59 \times E_G + 0.89 \times E_B = -0.89 \div 0.89$$

8.Digitization parameters, basic sampling formats and corresponding data rates for the TV signal

https://intranet.etc.upt.ro/~AVS/Course/4.5_E_DTV_web.pdf, 3-5, 12, 13

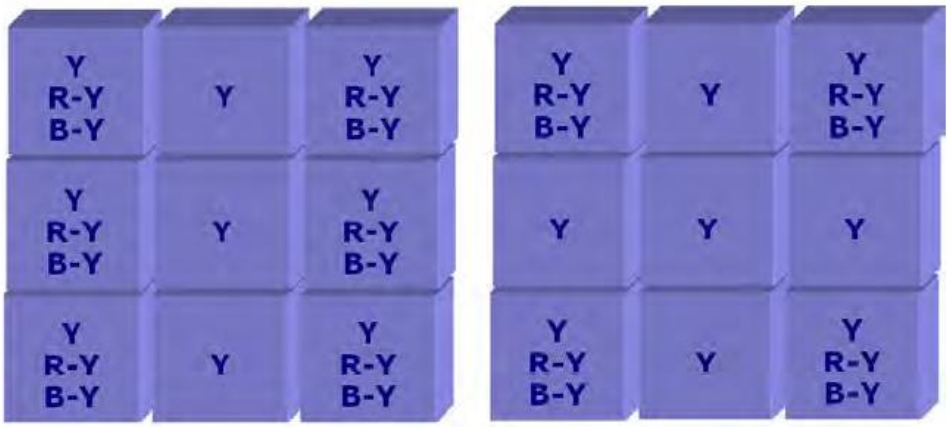
Digital TV studio standard (I+II+III)

- 1982, CCIR Rec.601 – **USA/Europe** standard
  - NTSC / SECAM / PAL
  - 525 / 625 lines
  - common **digital TV line**
    - same bit **rate**
    - same quality
    - easy system conversion
- TV components (**Y**, **R-Y**, **B-Y**)
  - **orthogonal** sampling
  - standard sampling frequency
    - f_S **= 13,5 MHz**
  - PCM format
    - **8 bits** / component sample



4:2:2 format

STUDIO quality



Digital television signal bit rate

- Digital signal bit rate
  - $D = f_S \times n$ [bits/s]
- TV signal bit rate
  - $D = D_Y + D_{R\text{-}Y} + D_{B\text{-}Y}$

    $= f_{S\,Y} \times n_Y + f_{S\,R\text{-}Y} \times n_{R\text{-}Y} + f_{S\,B\text{-}Y} \times n_{B\text{-}Y}$
- 4:2:2 format - TV signal bit rate
  - D_{TV} = 13.5 MHz × 8 b + 6.75 MHz × 8 b + 5.75 MHz × 8 b =

    = 108 Mbits/s + 54 Mbits/s + 54 Mbits/s = **216 Mbits/s**

Digital television standard family

	Standard	Parameters	D_Y	$D_{R\text{-}Y}+D_{B\text{-}Y}$	D [Mbps]
HIGHER ORDER FORMATS	4:4:4 progressive	f_H = 31.250 Hz f_S = 27 MHz	216	216+216	648
	4:4:4 interlaced	f_H = 15.625 Hz f_S = 13,5 MHz	108	108+108	324
BASIC FORMAT	4:2:2 studio	f_{SY} = 13,5 MHz f_{SC} = 6,75 MHz	108	54 + 54	216
LOWER ORDER	4:1:1	f_{SY} = 13,5 MHz f_{SC} = 3,375 MHz	108	27 + 27	162

FORMATS	4:2:0 broadcast	alternative on lines	4:2:2 4:0:0	108	54 + 54 0 + 0	162
	2:1:1	f_{SY} = 6,75 MHz f_{SC} = 3,375 MHz		54	27 + 27	108

9. The principle of MPEG compression

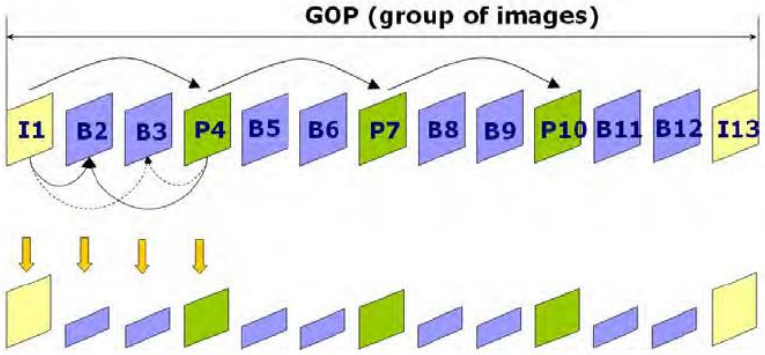
https://intranet.etc.upt.ro/~AVS/Course/4.6_E_MPEG_web.pdf, 7-9

MPEG coding (I+II)

- **Spatial** redundancy removal
  - DCT
- **Temporal** redundancy removal
  - Motion-compensated forward
  - Bidirectional prediction (interpolation)
- MPEG uses three **types of images**
  - **Image I**
    - **JPEG** coded
    - independent to the sequence of moving images
    - **robust** coding
    - independent to precedent errors
    - **low** compression factor

- **Image P**
  - a **predicted** image is estimated (motion-compensated forward)
  - the **difference** between actual and predicted image is **coded**
  - sequence of predictions may propagate possible **errors**
  - **higher** compression factor
- **Image B**
  - a bidirectional **interpolated** image is calculated, using I and P images
  - very good estimation
  - may propagate **errors**
  - **best** compression factor

Moving pictures digital compression (I)



Compression

- Different techniques are used
- Resulting different factors

10. The structure and the parameters of a TV channel

https://intranet.etc.upt.ro/~AVS/Course/4.4_E_RF_web.pdf, 3, 5

Modulation methods

- Amplitude modulation
  - **AM**

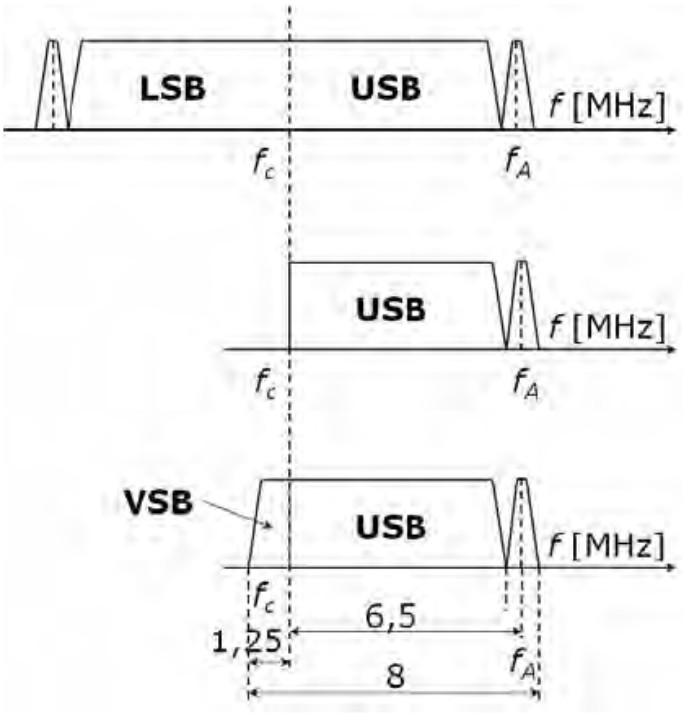
  ⇨low power efficiency

- Single Side Band AM
  - **SSB-AM**

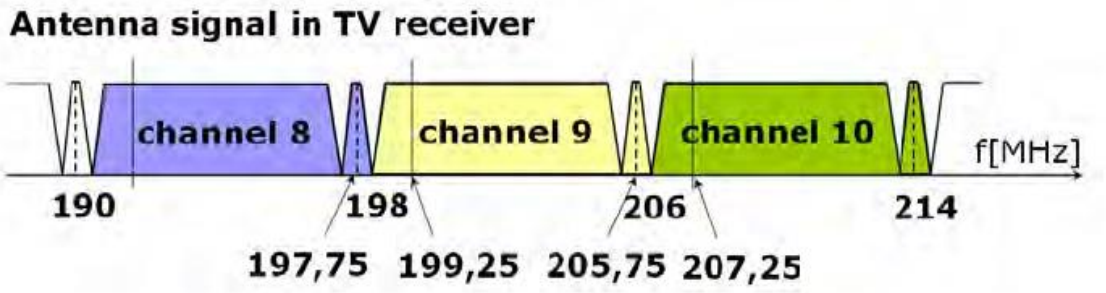
  ⇨impossible to filter

- Vestigial Side Band AM
  - **VSB-AM**

  ⇨standard solution

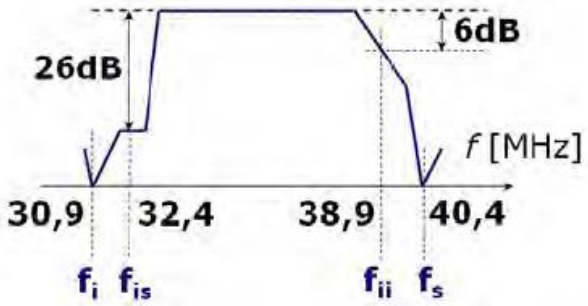


Intermediate frequency processing



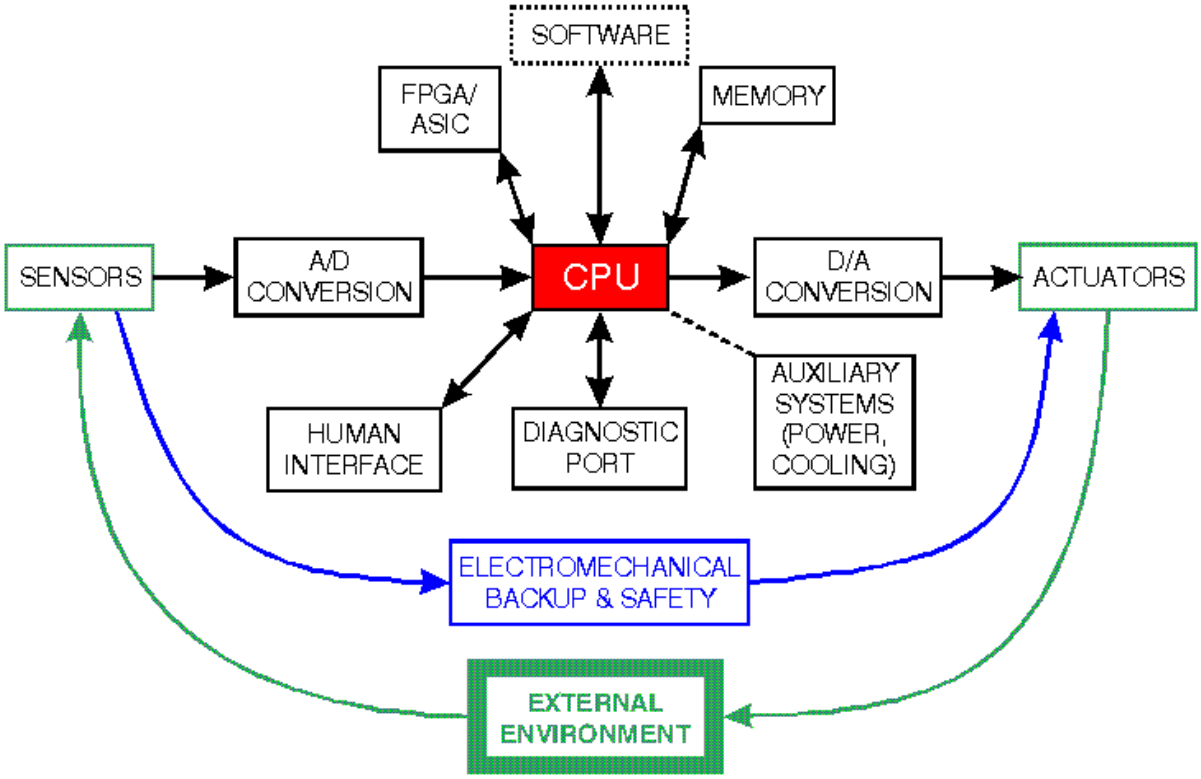
A **single filter** for:

- channel **extraction**
- adjacent channel **rejection**
- **VSB** rejection



1. The general architecture of an embedded system.

Answer: C.-D. Căleanu, Embedded Systems. Course Notes, 2011
https://intranet.etc.upt.ro/~EMBEDDED_SYS/Course , CHAPTER 1 slide 21.



2. What are the relative advantages/disadvantages of RISC versus CISC architectures?

Answer: C.-D. Căleanu, Embedded Systems. Course Notes, 2011
https://intranet.etc.upt.ro/~EMBEDDED_SYS/Course , CHAPTER 3, slides 13-15.

- The most common types of general-purpose ISA architectures implemented in embedded processors are:
- Complex Instruction Set Computing (CISC) Model
- Reduced Instruction Set Computing (RISC) Model

Complex Instruction Set Computing (CISC) Characteristics:

- A large number of instructions each carrying out different permutation of the same operation
- Instructions provide for complex operations
- Different instructions of different format
- Different instructions of different length
- Different addressing modes

- Requires multiple cycles for execution

Reduced Instruction Set Computing (RISC) Characteristics:

- Fewer instructions aiming simple operations that can be executed in a single cycle
- Each instruction of fixed length – facilitates instruction pipelining
- Large general purpose register set – can contain data or address
- Load-store Architecture – no memory access for data processing instructions

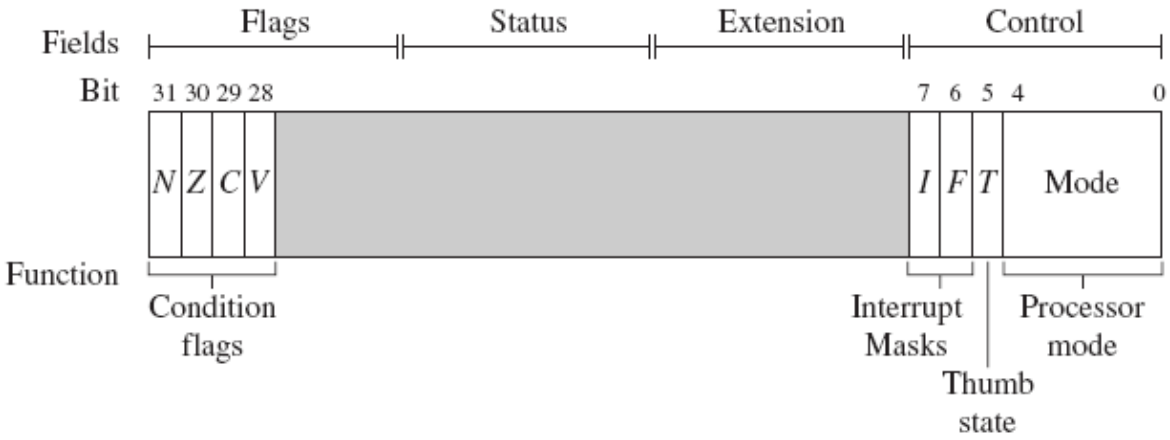
3. Enounce and explain the role of the following ARM registers: r13, r14 and r15, status registers.

Answer: C.-D. Căleanu, Embedded Systems. Course Notes, 2011
https://intranet.etc.upt.ro/~EMBEDDED_SYS/Course , CHAPTER 4, slide 17, 21

Three registers r13, r14, r15 perform special functions:
r13 – stack pointer,
r14 – link register where return address is put whenever a subroutine is called,
r15 – program counter

In addition, there are two status registers
- CPSR: current program status register
- SPSR: saved program status register

CPSR: monitors and control internal operations

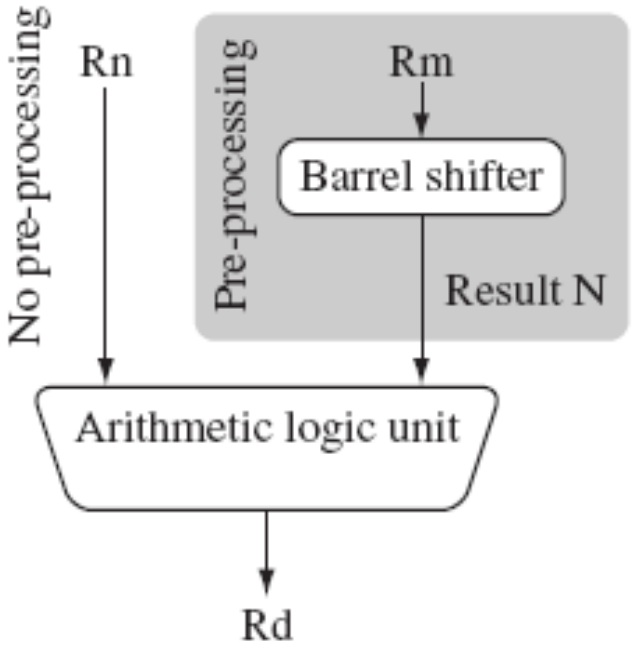


The top four bits of the CPSR contain the condition codes which are set by the CPU. The condition codes report the result status of a data processing operation. From the condition codes you can tell if a data processing instruction generated a negative, zero, carry or overflow result.
The lowest eight bits in the CPSR contain flags which may be set or clear ed by the application code. Bits 7 and 8 are the I and F bits. These bits are used to enable and disable the two interrupt sources which are external to the ARM7 CPU. Most peripherals are connected to these two interrupt lines. You should be careful when programming these two bits because in order to disable either interrupt source the bit must be set to '1' not '0' as you might expect. Bit 5 is the THUMB bit.

4. Which is the role of the barrel shifter? Present its block diagram and enumerate the basic operations which could be performed with it. Illustrate the concept with an assembly language example.

Answer: C.-D. Căleanu, Embedded Systems. Course Notes, 2011
https://intranet.etc.upt.ro/~EMBEDDED_SYS/Course , CHAPTER 4, slide 43, 44.

Enables shifting 32-bit operand in one of the source registers left or right by a specific number of positions within the cycle time of instruction
Basic Barrel shifter operations: Shift left, right, rotate
Facilitates fast multiply, division and increases code density
Example: mov r7, r5, LSL #2 - Multiplies content of r5 by 4 and puts result in r7



5. Present possible implementations for the non-volatile memory. What could be store in it?

Answer: C.-D. Căleanu, Embedded Systems. Course Notes, 2011
https://intranet.etc.upt.ro/~EMBEDDED_SYS/Course , CHAPTER 5, slide 10-12.

- Mask ROM
  - Used for dedicated functionality
  - Contents fixed at IC fab time (truly write once!)
- ERPOM (erase programmable)
  - Requires special IC process (floating gate technology)
  - Writing is slower than RAM, EPROM uses special programming system to provide special voltages and timing
  - Reading can be made fairly fast
  - Rewriting is slow
    - Erasure is first required, EPROM – UV light exposure, EEPROM – electrically erasable
- Flash

  - Uses single transistor per bit (EEPROM employs two transistors)
  - A flash memory provides high density storage with speed marginally less than that of SRAM's
  - Write time is significantly higher compared to DRAM
- On-chip non-volatile storage is used for storage of:
  - Configuration information
  - Executable code that runs on core processors
  - Recorded data: repeated write

6. The I2C protocol (features, connections, advantages, disadvantages).

Answer: C.-D. Căleanu, Embedded Systems. Course Notes, 2011
https://intranet.etc.upt.ro/~EMBEDDED_SYS/Course , CHAPTER 6, slide 21, 22, 25.

I2C Features:
- Bi-directional
  - Data can flow in both directions
- Synchronous (2 wires)
  - Data is clocked along with a clock signal
  - Clock signal controls when data is changed and when it should be read. Clock rate can vary unlike asynchronous (RS-232 style) communication
- I2C bus has three speeds:
  - Slow (under 100 Kbps)
  - Fast (400 Kbps)
  - High-speed (3.4 Mbps) – I2C v.2.0

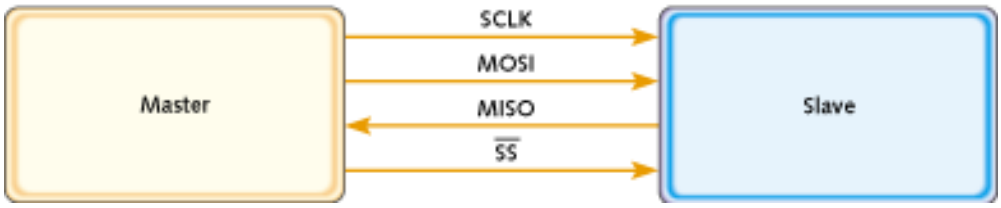
I2C Connections:
- Two wired bus
  - Serial DAta (SDA) line
  - Serial CLock (SCL) line
- Voltage Levels
  - High -1
  - Low - 0
- Bit transfer
  - SCL = 1 implies SDA = valid data
  - Stable data during high clock
  - Data change during low clocks

I2C Tradeoffs:
- Advantages:
  - Good for communication with on-board devices that are accessed occasionally
  - Easy to link multiple devices because of addressing scheme
  - Cost and complexity do not scale up with the number of devices
- Disadvantages:
  - The complexity of supporting software components can be higher than that of competing schemes (for example, SPI)

7. The SPI protocol (bus configuration, comparison with I2C).

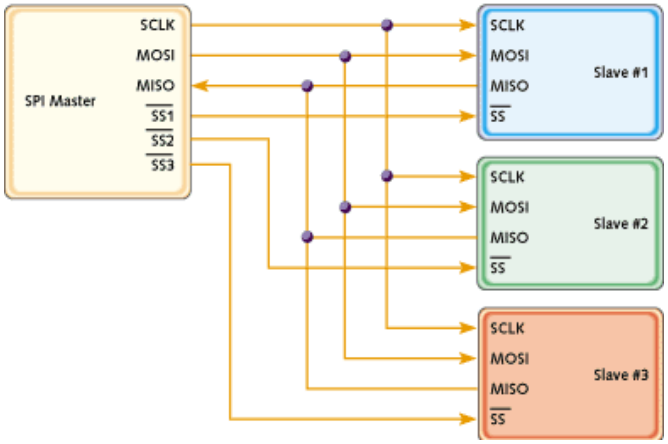
Answer: C.-D. Căleanu, Embedded Systems. Course Notes, 2011
https://intranet.etc.upt.ro/~EMBEDDED_SYS/Course , CHAPTER 6, slide 27, 28.

SPI Bus Configuration



- Synchronous serial data link operating at full duplex
- Master/slave relationship
- 2 data signals:
  - MOSI – master data output, slave data input
  - MISO – master data input, slave data output
- 2 control signals:
  - SCLK – clock
  - /SS – slave select (no addressing)

SPI vs. I^2C



- For point-to-point, SPI is simple and efficient
  - Less overhead than I2C due to lack of addressing, plus SPI is full duplex.
- For multiple slaves, each slave needs separate slave select signal
  - More effort and more hardware than I2C

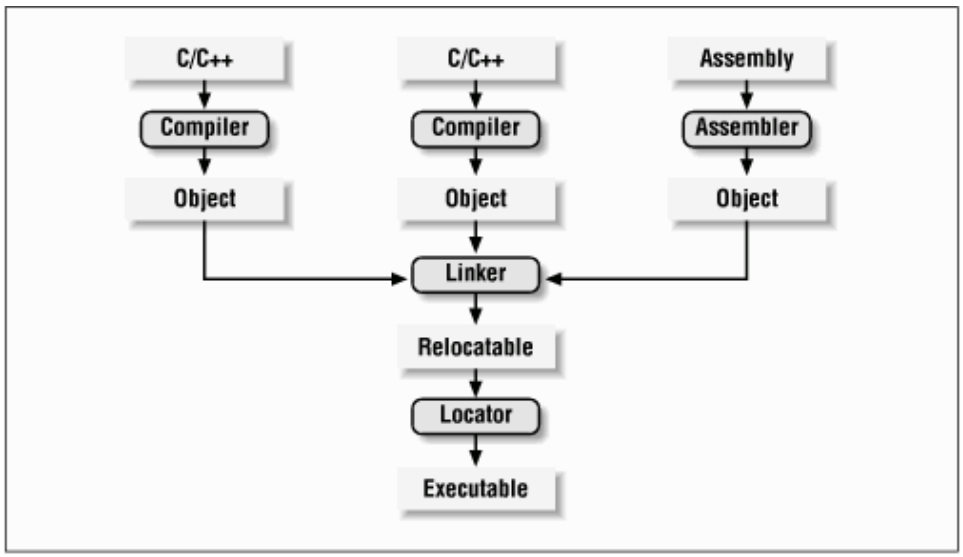
8. Enumerate the functions of the start-up code.

Answer: C.-D. Căleanu, Embedded Systems. Course Notes, 2011
https://intranet.etc.upt.ro/~EMBEDDED_SYS/Course , CHAPTER 7, slide 20.

- Start-up code usually consists of the following actions in sequence:
  - Disable all interrupts
  - Copy any predefined data from ROM to RAM
  - Zero the uninitialized data area
  - Allocate space and initialize the stack
  - Initialize processor's SP
  - Create and initialize the heap
  - Possibly execute constructors and initializers for global variables for object oriented languages like C++
  - Enable interrupts
  - Call main

9. Enounce the typical steps involved in the software building process.

Answer: C.-D. Căleanu, Embedded Systems. Course Notes, 2011
https://intranet.etc.upt.ro/~EMBEDDED_SYS/Course , CH. 7, slide 25.



10. Define the kernel and its responsibilities.

Answer: C.-D. Căleanu, Embedded Systems. Course Notes, 2011
https://intranet.etc.upt.ro/~EMBEDDED_SYS/Course , CH. 8, slide 12, 13.

Kernel's definition

- Most frequently used portion of OS
- Resides permanently in main memory
- Runs in privileged mode
- Responds to calls from processes and interrupts from devices

Kernel’s responsibility

- Managing Processes
- Context switching: alternating between the different processes or tasks
    - Various scheduling algorithms
    - Scheduling: deciding which task/process to run next
- Various solutions to dealing with critical sections
    - Critical sections = providing adequate memory-protection when multiple tasks/processes run concurrently