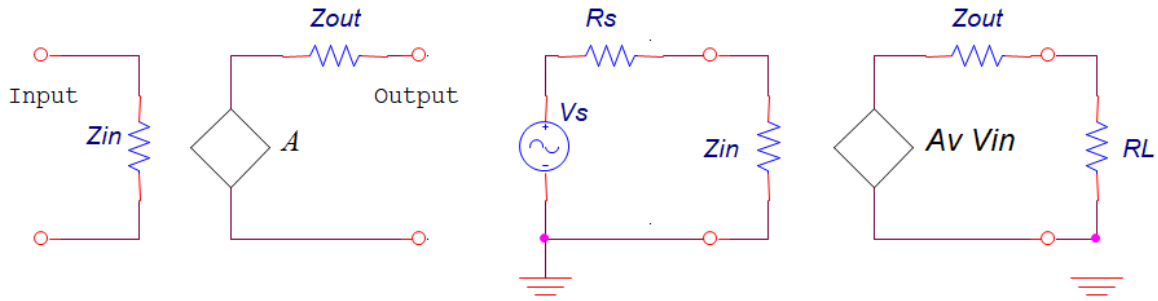


## Electronic Circuits - Theory

1. Demonstrate the optimum input and output impedance for a voltage amplifier.

### Demonstration:



### Amplifier model

### Amplifier circuit

- At the circuit input and output there are 2 voltage dividers:

$$V_{in} = V_s \frac{Z_{in}}{R_s + Z_{in}} \quad V_L = V_{out} \frac{R_L}{Z_{out} + R_L}$$

where  $v_{out} = A_V v_{in}$

- Since  $v_{in} < v_s$  and  $v_L < v_{out}$ ,  
 $\Rightarrow$  The *effective voltage gain* of a circuit is lower than the calculated voltage gain of the amplifier itself.

To neglect the input and output voltage drop we want :

[Infinite gain], Infinite input impedance, Zero output impedance  $\Rightarrow$  the ideal voltage amplifier

2. Explain Miller effect and theorem and its utility for high frequency analysis.

### Answer:

An impedance  $Z_{12}$  connected from the input of an amplifier to the output can be replaced by an impedance across the input terminals ( $Z_{10}$ ) and impedance across the output terminals ( $Z_{20}$ ).

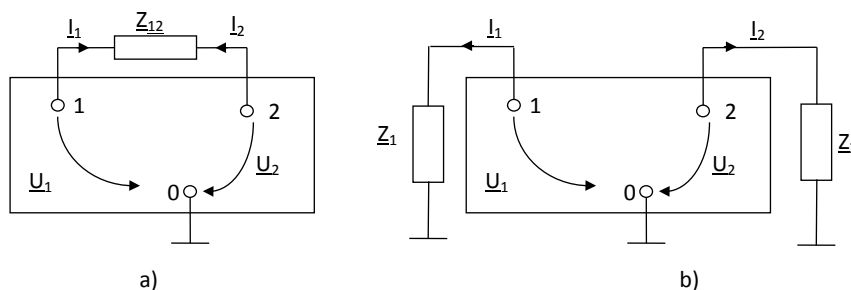


Fig.3

$$\begin{cases} Z_1 = Z_{12} \cdot \frac{1}{1-K} \\ Z_2 = Z_{12} \cdot \frac{1}{1-\frac{1}{K}} \end{cases} \quad \text{where } K = \frac{U_2}{U_1} \text{ is voltage gain at midband}$$

For a capacitor, considering:  $\left( Z_{12} = \frac{1}{j\omega C_{12}} \right)$

$$\begin{cases} C_{10} = C_{12}(1 - K) \\ C_{20} = C_{12}\left(1 - \frac{1}{K}\right) \end{cases}$$

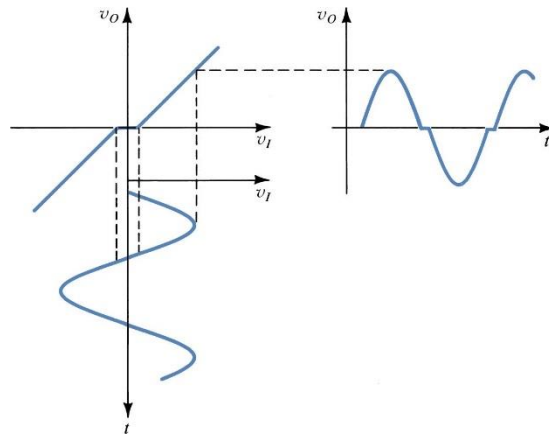
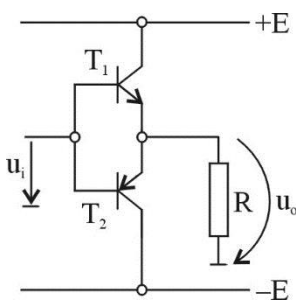
Miller Theorem can be used in high-frequency circuit analysis in order to eliminate feedback capacitances, admitting that  $K$  is computed at midband frequency, thus ignoring the zeros from the complex transfer function. Due to the fact that feedback impedances are removed, the equivalent circuit is simplified if Miller is used.

3. Which amplifier class is known for its crossover distortions? Explain the root cause and ways of improvement based on a simplified schematic and its transfer characteristic.

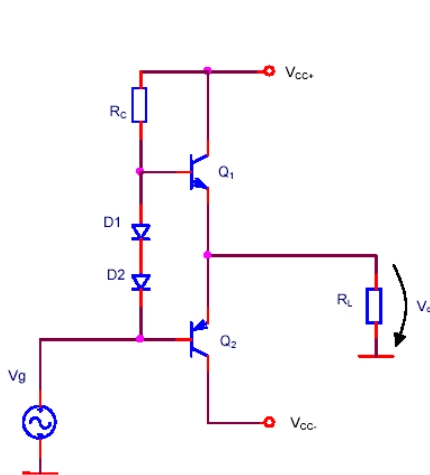
Answer:

Class B amplifier (Push pull) has cross over distortions due to an input voltage range where both transistors are not in conduction.

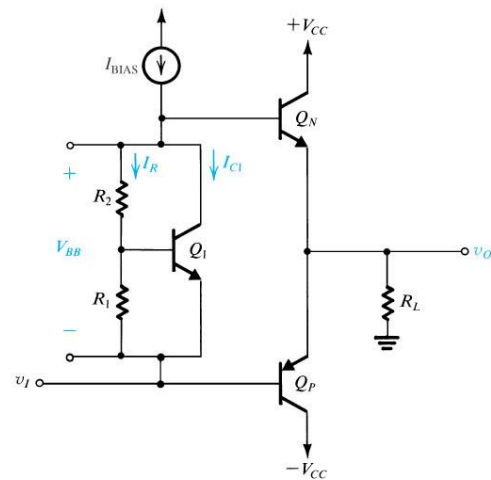
Conduction angle of each transistor is less than  $\frac{1}{2} T$ , resulting in crossover distortion between the “halves” of the signal



Distortions are reduced if a biasing circuit (i.e with 2 diodes or a “Vbe multiplier”) is used to keep transistors closer to conduction when they are in steady state:



Biasing with diodes



Biasing with Vbe multiplier

4. Demonstrate bandwidth extension for an amplifier when a negative feedback is applied.

Answer:

When a negative feedback is used, both low and high cut off frequencies are shifted as follow:

At high frequency (considering an amplifier with one pole):

$$\text{EX 1 : } A(j\omega) = \frac{A_0}{1 + j \frac{f}{f_i}} \quad \beta = \beta_0$$

$$A_r(j\omega) = \frac{\frac{A_0}{1 + j \frac{f}{f_i}}}{1 + \frac{\beta_0 A_0}{1 + j \frac{f}{f_i}}} = \frac{A_0}{1 + \beta_0 A_0 + j \frac{f}{f_i}} = \frac{A_0}{1 + \beta_0 A_0} \cdot \frac{1}{1 + j \frac{f}{f_i(1 + \beta_0 A_0)}} = A_{r0} \cdot \frac{1}{1 + j \frac{f}{f_{ir}}}$$

$$A_{r0} = \frac{A_0}{1 + \beta_0 A_0} \quad \text{si } f_{ir} = f_i(1 + \beta_0 A_0)$$

$$A_r = \frac{A}{F} ; f_{ir} = f_i F ; A_r \cdot f_{ir} = A \cdot f_i$$

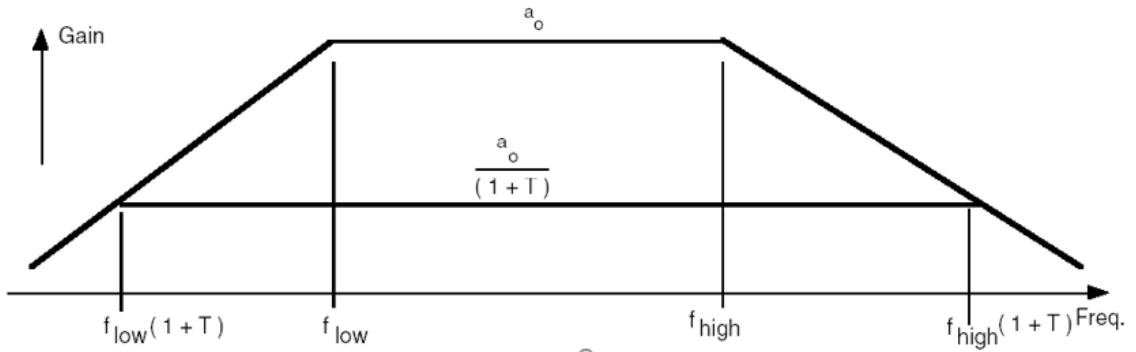
At low frequency:

$$\text{EX2 : } A(j\omega) = A_0 \cdot \frac{j \frac{f}{f_j}}{1 + j \frac{f}{f_j}} \quad \beta = \beta_0$$

$$A_r(j\omega) = \frac{j \frac{f}{f_j} A_0}{1 + j \frac{f}{f_j} + j \frac{f}{f_j} \beta_0 A_0} = \frac{j \frac{f}{f_j} A_0}{(1 + \beta_0 A_0) j \frac{f}{f_j} + 1} = \frac{A_0}{1 + \beta_0 A_0} \cdot \frac{j \frac{f}{f_j} (1 + \beta_0 A_0)}{1 + j \frac{f}{f_j} (1 + \beta_0 A_0)} = A_{r0} \cdot \frac{j \frac{f}{f_{jr}}}{1 + j \frac{f}{f_{jr}}}$$

$$f_{jr} = \frac{f_j}{1 + \beta_0 A_0}$$

$$A_r = \frac{A}{F} \quad f_{jr} = \frac{f_j}{F}$$



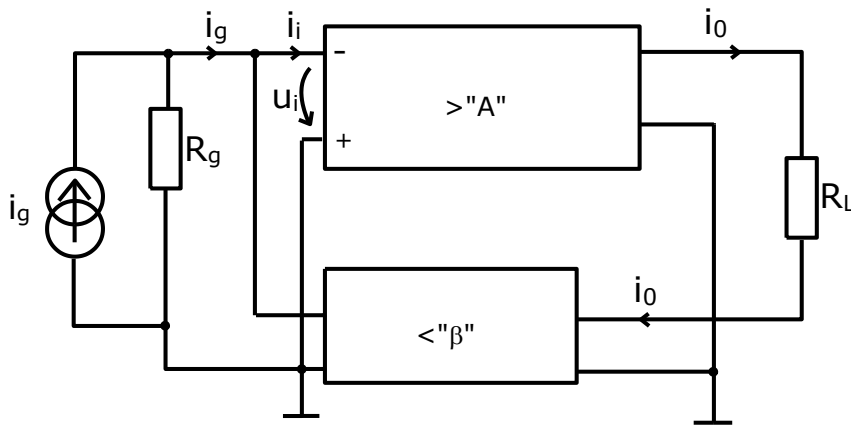
The bandwidth  $BW = f_{high} - f_{low}$  is thus extended.

It can be considered that  $G \cdot BW = ct$ , a relation that shows that bandwidth can be increased with the same factor as gain is decreased

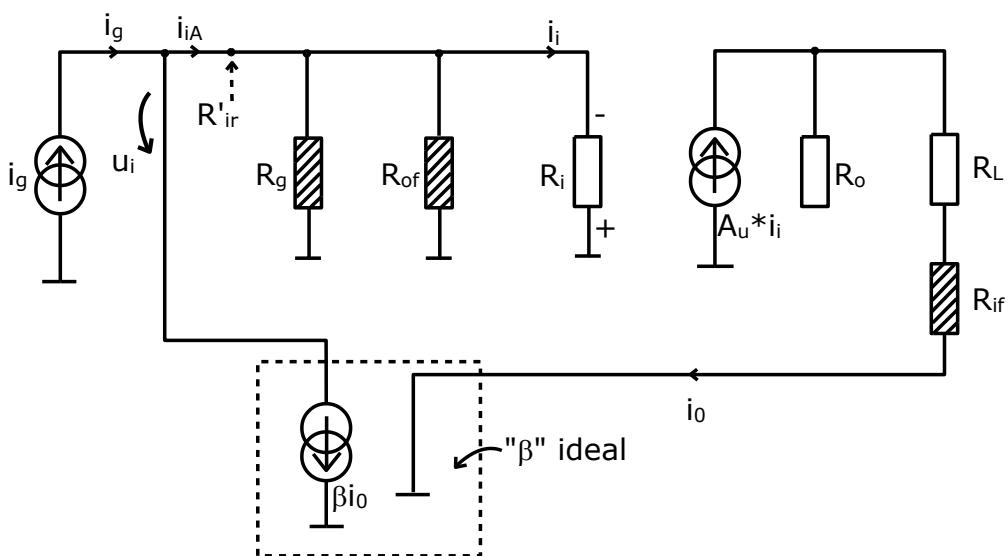
5. Show input and output resistance change for an amplifier when a shunt-series feedback is applied. Justify with formulas.

Answer:

Topology of shunt-series feedback:



Equivalent schematic at midband:



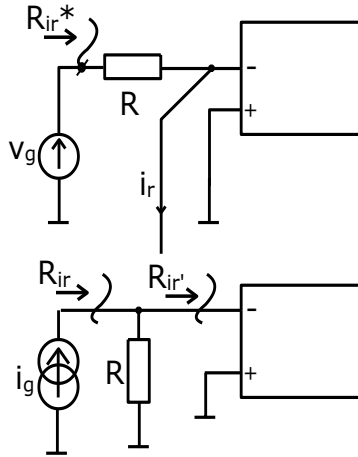
Input resistance with feedback:

$$R_{ir} = \frac{u_i}{i_g}$$

$$i_g = i_r + i_{iA} = \beta \cdot i_0 + i_{iA} =$$

$$\beta \cdot A_{iA} \cdot i_{iA} + i_{iA} = (1 + \beta \cdot A_{iA}) i_{iA}$$

$$= (1 + \beta A_{iA}) \cdot \frac{u_i}{R_g \parallel R_{of} \parallel R_i}$$



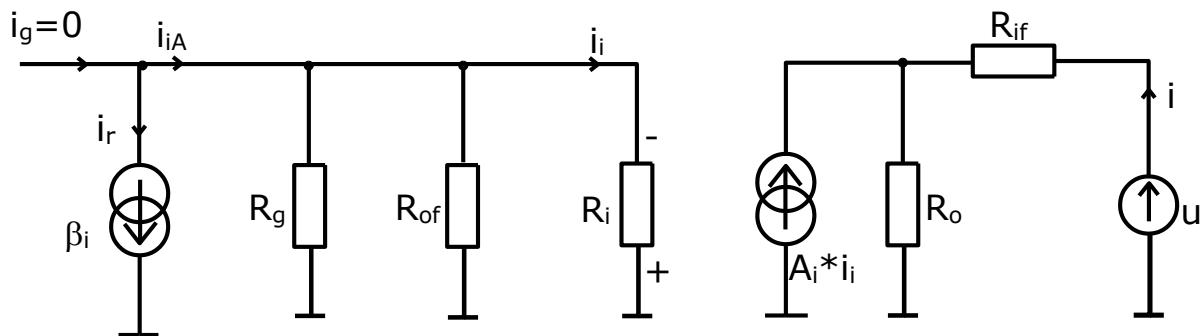
$$R_{ir} = \frac{u_i}{i_g} = \frac{R_{iA}}{1 + \beta A_{iA}}$$

$$R_{ir} = R \parallel R_{ir}' \cong R_{ir}'$$

$$R_{ir}^* = R + R_{ir}' \cong R$$

Input resistance is increased at the amplifier input, but the input signal generator must consider also the resistance outside the feedback loop, that most of the time “dictate” the value of the real input resistance.

Output resistance with feedback is determined without input signal and load replaced with a test voltage source:



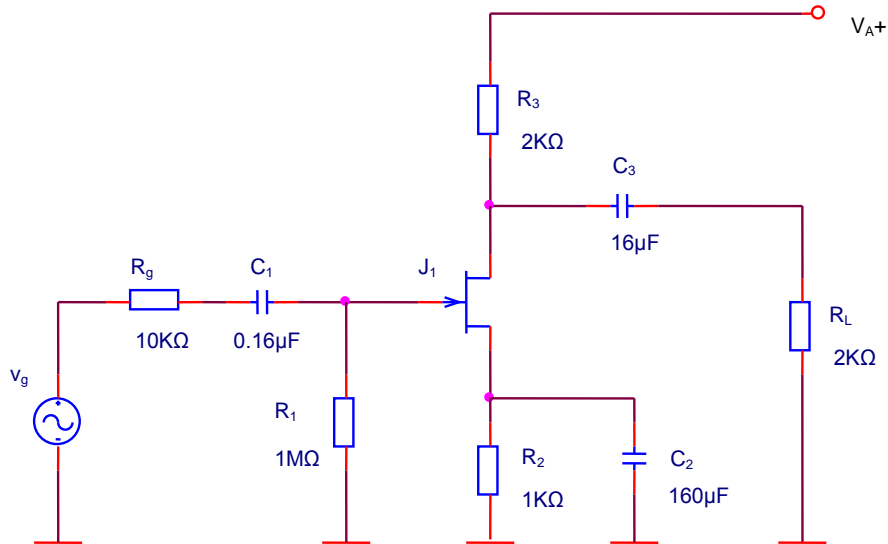
$$R_{oA} = R_o + R_{if}$$

$$R_{or} = R_{oA} (1 + \beta (A_{iA})_{R_L=0})$$

Output resistance is increased due to series sampling.

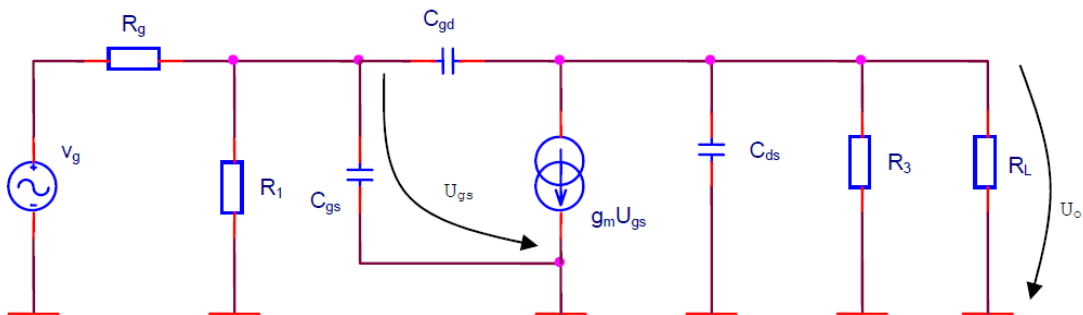
## Electronic Circuits - Problems

- For the circuit below, having the J-FET with parameters:  $g_m = 5\text{mA/V}$ ,  $r_{ds} = \infty$ ,  $C_{gd} = 5\text{pF}$ ,  $C_{gs} = 10\text{pF}$ ,  $C_{ds} = 10\text{pF}$ . Find out the high cutt off frequency by:
  - Using Miller Theorem;
  - Using OCTC (Open Circuit Time Constant) method.

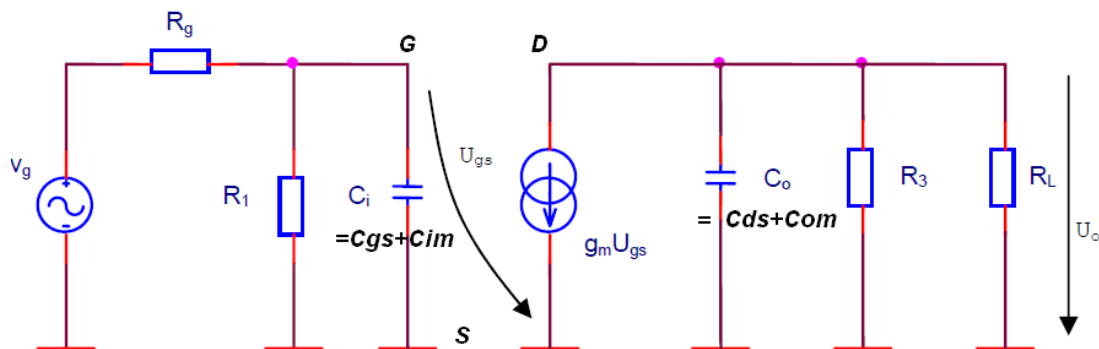


### Solution:

- First must draw equivalent schematic for small signal, mean frequencies:



By using Miller theorem,  $C_{gd}$  can be splitted in 2 capacitors to ground  $C_{im}$  and  $C_{om}$ , which will add to existing  $C_{gs}$  respective  $C_{ds}$ , resulting in  $C_i$  and  $C_o$  as below:



Gain  $K$  between  $G$  and  $D$  is needed to estimate  $C_{im}$  and  $C_{om}$  capacitances:

$$K = \frac{U_o}{U_i} \text{ si } U_o = -g_m U_{gs} (R_3 \parallel R_L), U_i = U_{gs} \Rightarrow K = A_{U0} = -g_m R_3 \parallel R_L = -5$$

Then according to Miller:

$$C_{iM} = C_{gd}(1-K) = 30 \text{ pF}, C_{oM} = C_{gd} \left(1 - \frac{1}{K}\right) = 6 \text{ pF}$$

$$C_i = C_{gs} \parallel C_{iM} = C_{gs} + C_{iM} = 40 \text{ pF}, C_o = C_{ds} \parallel C_{oM} = C_{ds} + C_{oM} = 16 \text{ pF}$$

Cutt of (pole) frequencies introduced by these capacitors are:

$$f_{P1} = \frac{1}{2 \cdot \pi \cdot C_i \cdot R_{P1}}, R_{P1} = R_g \parallel R_1 \cong R_g \cong 10 \text{ K}\Omega \Rightarrow f_{P1} = 400 \text{ KHz}$$

$$f_{P2} = \frac{1}{2 \cdot \pi \cdot C_o \cdot R_{P2}}, R_{P2} = R_3 \parallel R_L = 1 \text{ K}\Omega \Rightarrow f_{P2} = 10 \text{ MHz}$$

Transfer function by neglecting zero frequency introduced by  $C_{gs}$  will be:

$$A_U(j\omega) = -5 \cdot \frac{1}{\left(1 + j \frac{f}{0.4 \cdot 10^6}\right) \cdot \left(1 + j \frac{f}{10 \cdot 10^6}\right)}$$

High cutt of frequency will have aproximative value:

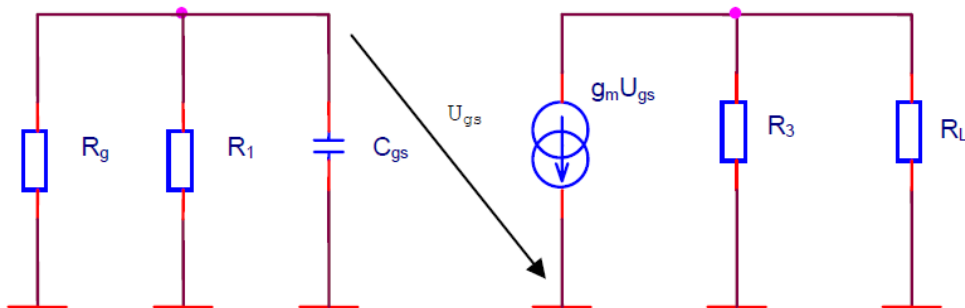
$$f_{P1} = 400 \text{ KHz}$$

Or can be computed exactly considering the 3db attenuation at cutt of frequency:

$$\left|A_U(j\omega)\right|_{f=f_i} = \frac{1}{\sqrt{2}} A_{U0} \Rightarrow f_i = 393,7 \text{ KHz}$$

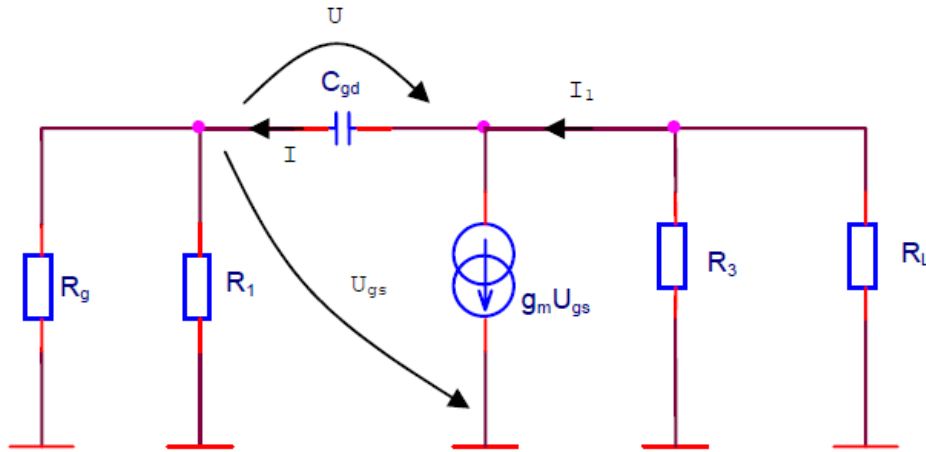
b) If OCTC is applied to first schematic (without to get benefit of Miller theoreme), involve to evaluate 3 time constants, one for each capacitor as folows:

➤ **C<sub>gs</sub> effect**, all the others C = open circuit:



$$f_{P1} = \frac{1}{2 \cdot \pi \cdot C_{gs} \cdot R_{P1}}, R_{P1} = R_1 \parallel R_g \cong R_g \cong 10 \text{ K} \Rightarrow f_{P1} = 1,6 \text{ MHz}$$

➤ **C<sub>gd</sub> effect**, all the others C = open circuit:



$$f_{P2} = \frac{1}{2 \cdot \pi \cdot C_{gd} \cdot R_{P2}}$$

Equivalent resistance between \$C\_{gd}\$ nodes can be found if \$C\_{gd}\$ is replaced with a voltage source \$U\$:

$$R_{P2} = \left| \frac{U}{I} \right|$$

Using Kirchhoff laws :

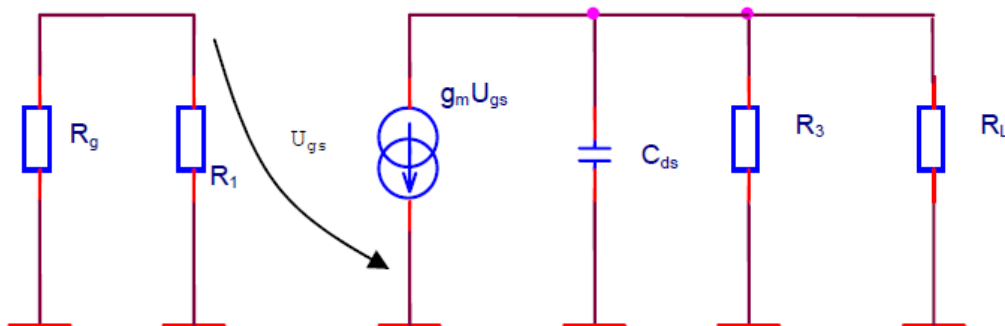
$$-i \cdot R_g \parallel R_1 + u_{gs} = 0 \Rightarrow u_{gs} = i \cdot R_g \parallel R_1$$

$$I_1 = g_m \cdot u_{gs} + I = I(1 + g_m \cdot R_g \parallel R_1)$$

$$U - I \cdot R_g \parallel R_1 - I_1 \cdot R_3 \parallel R_L = 0 \Rightarrow U = I \cdot R_g \parallel R_1 + I \cdot (1 + g_m \cdot R_g \parallel R_1) \cdot R_3 \parallel R_L$$

$$R_{P2} = \frac{U}{I} = R_g \parallel R_1 + (1 + g_m \cdot R_g \parallel R_1) \cdot R_3 \parallel R_L = 61K\Omega \Rightarrow f_{P2} = 524,6KHz$$

➤ **Cds effect**, all the others \$C = \text{open circuit}\$:



$$f_{P3} = \frac{1}{2 \cdot \pi \cdot C_{ds} \cdot R_{P3}}, \quad R_{P3} = R_3 \parallel R_L = 1K \Rightarrow f_{P3} = 16MHz$$

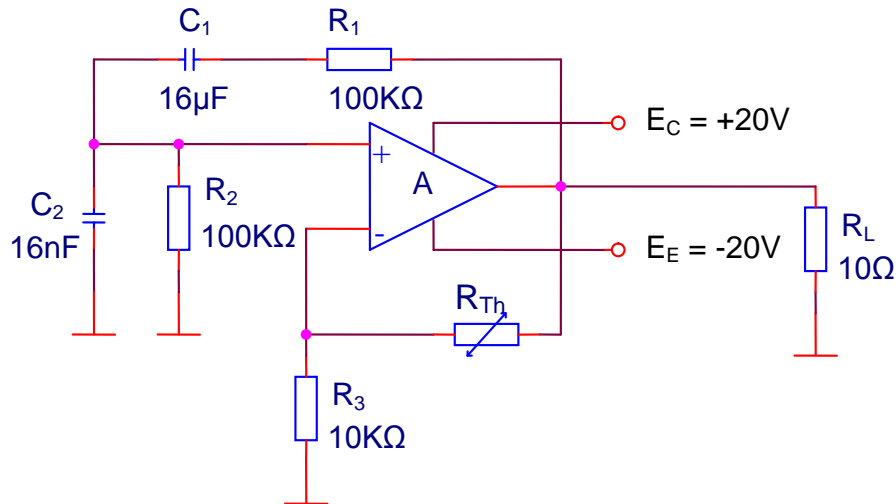
According to SCTC:

$$\frac{1}{f_i} = \frac{1}{f_{i1}} + \frac{1}{f_{i2}} + \frac{1}{f_{i3}} \Rightarrow f_i \cong 385,2KHz.$$



close to the value obtained at a)

2. The schematic below is a Wien oscillator using a class B final stage amplifier having:  
 $A_u \rightarrow \infty$ ,  $R_i \rightarrow \infty$ ,  $R_o \rightarrow 0$ . Find out:  
 a)  $f_o$  oscillating frequency,  
 b)  $V_o$ , when using the thermistor  $R_{Th}$ ;  
 c)  $P_o$  (delivered to  $R_L$ )



**Solution:**

a)  $f_o = \frac{1}{2 \cdot \pi \cdot \sqrt{R_1 R_2 C_1 C_2}} \cong 100Hz$

b)  $A = 1 + R_{Th}/R_3$ , and at  $f_o$ :  $|\beta| = 1/3$ .

From  $|A||\beta| = 1 \Rightarrow R_{Th} = 20k\Omega$  obtained for  $U_{Th} = 10V$ .

Feedback topology is series-shunt, actually a voltage divider including  $R_{Th}$ , so:

$$u_{R_{Th}} = u_o \cdot \frac{R_{Th}}{R_{Th} + R_3} = \frac{2}{3} \cdot u_o \Rightarrow u_o = 1,5 \cdot u_{R_{Th}} = 15V_{ef}$$

$$u_{om} = \sqrt{2} \cdot 15V_{vv}$$

c)

$$P_o = \frac{u_{om}^2}{2 \cdot R_L} = 22,5W$$

1) Explain how a decoder can be used as a demultiplexer.

D	CLK	Q
---	-----	---

decoder can be used as demultiplexer.

Any binary decoder can be used as a

with an enable input demultiplexer. The

decoder's enable input is connected to the data line and its select inputs determine which of the output lines is driven with the data bit. The following example shows how 74HC(T)138 can be used as demultiplexer.

If the decoder's enable input active HIGH ("1") is connected to the data line and the select inputs are  $A=C="1"$  and  $B="0"$  at the output Y5 one can find the data bit negated. The remaining output lines are "1" (see Fig.1.1.)

If the decoder's enable input active LOW ("0") is connected to the data line and the select inputs are  $A=C="1"$  and  $B="0"$  at the output Y5 one can find the data bit. The remaining output lines are "1" (see Fig.1.2.)

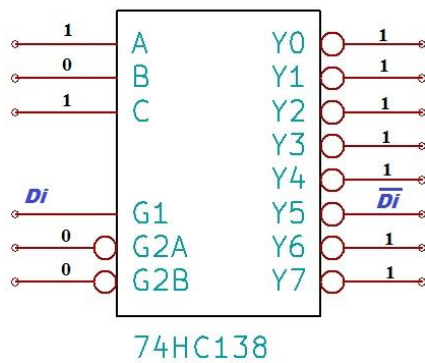


Fig. 1.1

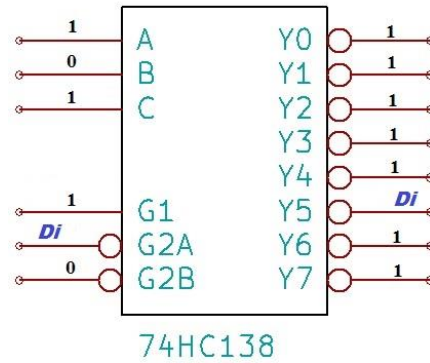


Fig. 1.2

2) Positive edge triggered D type flip-flop: draw a symbolic representation, the truth table and its associated waveforms

One of the simplest flip-flops which is produced on the market is the Positive – edge – triggered D flip-flop. This samples its D input and changes its  $Q$  and  $\bar{Q}$  outputs only on the rising edge of a controlling CLK signal (see Fig.

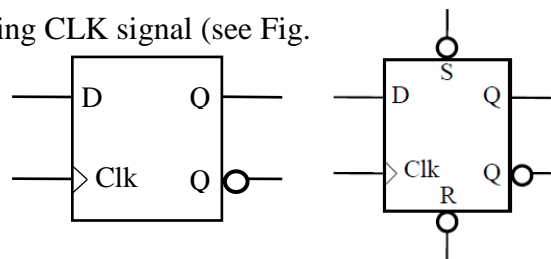


Fig. 2.1 a) Positive edge triggered D flip-flop b) Positive edge triggered D flip-flop with asynchronous inputs.

Table 1. Truth table for the D flip-flop

1	↑ edge	1
0	↑ edge	0
X	0	Last Q
X	1	Last Q

The edge-triggered D flip-flop has a setup and hold time window during which the D inputs must not change. This window occurs around the triggering edge of CLK, and is indicated by shaded color Fig 2.2.

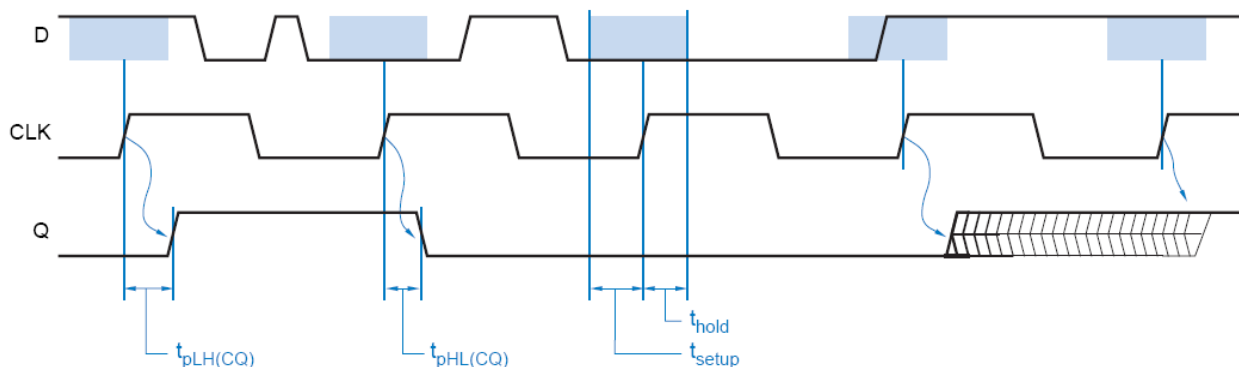


Fig. 2.2 Positive edge triggered D flip-flop waveforms

Some D flip-flops have *asynchronous inputs* (see Fig. 2.1. b) that may be used to force the flip-flop to a particular state independent of the CLK and D inputs, they are best reserved for initialization and testing purposes, to force a sequential circuit into a known starting state. If the asynchronous inputs are active LOW and S="0" and R="1" the output Q is "1", no matter what logic value is at the D input. If R="0" and S="1" the output is Q is "0", no matter what logic value is at the D input.

### 3) Sequential access memories FIFO and LIFO

A sequential memory is a memory in which the stored data cannot be read or written in random order, but must be addressed in a specific sequence. There are two main ways of organizing a sequential memory—as a **queue** or as a **stack**.

A queue is a **first-in first-out (FIFO)** memory, meaning that the data can be read only in the same order they are written. This memory can be implemented using SISO shift registers which can shift the data to the right.

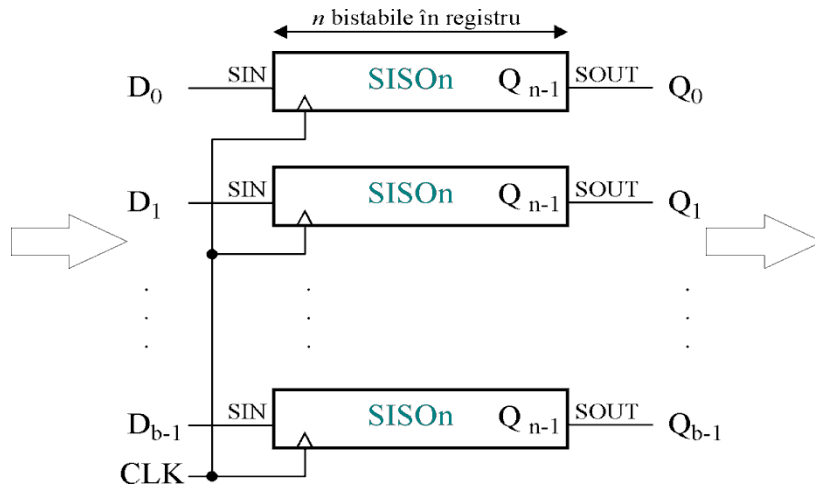


Fig. 5.1 Sequential memory

The binary words on  $b$  bit are written in parallel to the  $b$  serial inputs by applying a clock tick and shifting the data to the right. Once the words are written in the registers the first word to be read is the first one loaded in the memory. Once the data is read it is lost.

One common use for FIFO memory is to connect two devices that have different data rates. For instance, a computer can send data to a printer much faster than the printer can use it. To keep the computer from either waiting for the printer to print everything or periodically interrupting the computer's operation to continue the print task, data can be sent in a burst to a FIFO, where the printer can read them as needed.

The **last-in-first-out** (LIFO), or stack, is based on the following operation principle: the last bit to be written is the first bit to be read. This memory can be implemented using SISO shift registers which can shift the data bidirectional. To write the data the same principle from FIFO is used. To read the content of the memory, the data is shifted to the left.

The LIFO memory can be used for the storage of data that are to be retrieved in reverse order. Most microprocessors use a stack to save status flag bits and the contents of certain registers, in case of interruptions.

**4) 4-bit Up Binary Ripple Counter: draw the schematic, explain how it works, and draw the relevant waveforms**

A 4-bit up binary ripple counter build with 4 T flip-flops (from JK-MS with  $T = "1"$ ) can be seen in Fig 5. The clock ticks are applied only to the first flip-flop. The next flip-flops have as clock signal the output  $Q$  of the previous flip-flop (MR – Master Reset is synonym to R – Reset or CLR - Clear).

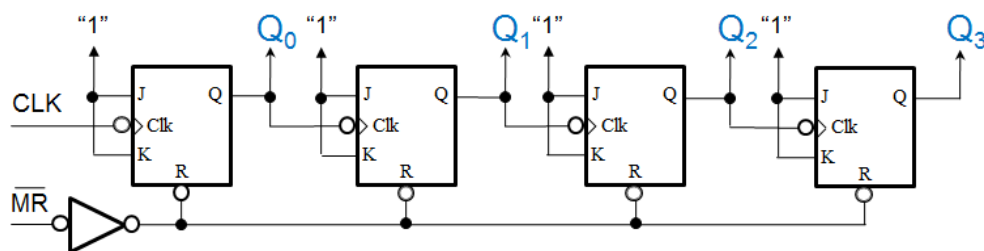


Fig 6.1. 4-bit Up Binary Ripple Counter

Notes:

- 1) The counter counts up, at each CLK tick the value of the counter is incremented with one unit.

2) The counter is modulus 16 (it has 4 flip-flops), the 16<sup>th</sup> tick of the clock close the cycle and brings the counter to zero. The 17<sup>th</sup> tick of the clock is the first tick from the next cycle.

3) At a certain moment of time, the binary code read at the outputs, corresponds to the number of ticks from that cycle (after 11 ticks  $Q_3Q_2Q_1Q_0 = 1011$  this corresponds to number 11 coded in binary). This is practically the counting function.

4) The flip-flops works as frequency dividers by 2. The output  $Q_0$  divides by 2 the clock signal,  $Q_1$  divides by 2 the frequency of the signal  $Q_0$  and by 4 the clock signal and so on.

5) In order to extend the modulus of the counter multiple counters can be cascade (the output  $Q_3$  is connected to the CLK input of the next counter).

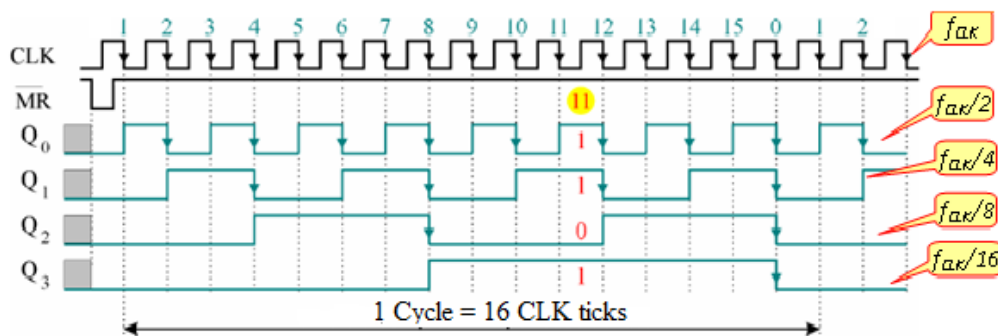


Fig 6.4. 4-bit Up Binary Ripple Counter waveforms

In order to get a countdown counter, the output  $\overline{Q}$  of the flip-flop is connected to the CLK input of the next flip-flop.

### 5) Shift Register Counters – Johnson Counter

A shift register can be combined with combinational logic to form a state machine whose state diagram is cyclic.

Such a circuit is called a *shift-register counter*. Unlike a binary counter, a shift-register counter does not count in an ascending or descending binary sequence, but it is useful in many “control” applications nonetheless.

An n-bit shift register with the complement of the serial output fed back into the serial input is a counter with  $2n$  states and is called a twisted-ring, **Moebius**, or **Johnson** counter.

The block diagram and the waveforms for a 4 bit Johnson counter are shown below. The decoded outputs are **glitch free**.

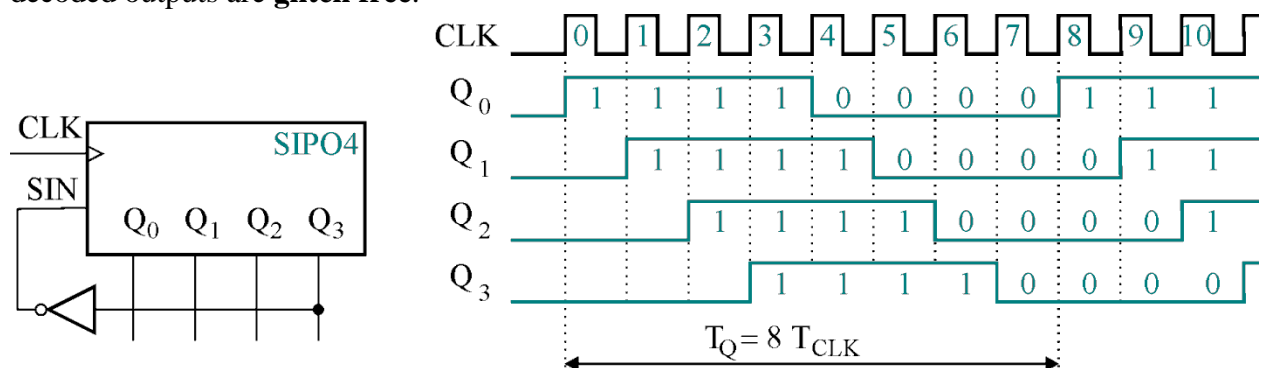


Fig. 9.1 Block diagram and the waveforms for a 4 bit Johnson counter

**1) Application Implement a modulo 51 counter.**

Let  $p=51$ . The number of flip-flops needed to implement it is  $n$ , where  $2^{n-1} < 51 < 2^n$ .  $n=6$  ( $32 < 51 < 64$ )

A modulo  $p = 51$  means resetting the counter after the 51<sup>st</sup> clock tick. This is done by identifying the state 51 with a circuit (an AND/NAND gate) and clear the counter by activating  $\overline{\text{CLR}}$ .

The truth table for the modulo 51 counter is shown below.

Table 11.1 Truth table for a modulo  $p=51$  counter

Clock tick	$Q_5$	$Q_4$	$Q_3$	$Q_2$	$Q_1$	$Q_0$
<b>0</b>	0	0	0	0	0	0
<b>1</b>	0	0	0	0	0	1
.						
<b>50</b>	1	1	0	0	1	0
<b>51 (0)</b>	1 → 0	1 → 0	<b>0</b>	<b>0</b>	1 → 0	1 → 0

A 4 input NAND gate is needed to detect the 51 state.

$$p = 51 = 1 \cdot 32 + 1 \cdot 16 + 0 \cdot 8 + 0 \cdot 4 + 1 \cdot 2 + 1 \cdot 1$$

The inputs of the gate are connected to the  $Q_5, Q_4, Q_1, Q_0$  outputs which are „1” logic only when the state 51 is detected. At that moment input  $\overline{\text{CLR}}$  is active (the output of the NAND gate is „0” only in this state) and clears the counter, so state 51 becomes state 0, in this way the number of distinct states of the counter is reduced to 51.

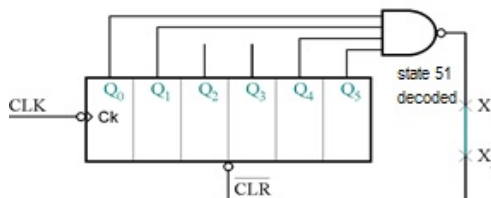


Fig 11.1 Decoding state 51

This schematic has an issue due to dispersion of the propagation times  $t_{\text{CLR-Q}}$ . The flip-flop with the shortest propagation time is clear first and its output  $Q$  (which is one of the inputs of the NAND gate) goes to "0". Thus, the gate output switches to "1" and interrupts the counter full reset process (other bistable will not be deleted).

To eliminate this disadvantage an /S-/R-flip-flop is used to hold the /CLR line active long enough time to clear all flip-flops but shorter than the clock pulse. The /S-/R-flip-flop is inserted between X1 and X2.

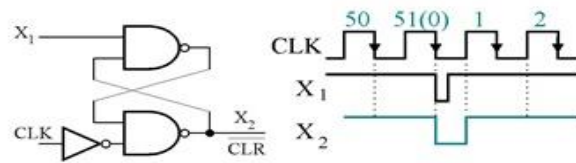


Fig. 11.2 Generating a proper clear signal

**2) Application Using semiconductor memory SRAM 6264 (8k x 8 bit) and a minimum number of logic circuits implement a 32k x 8 bit memory.**

First the number of circuits of type 6264 is determined.

$$N = \frac{32k \times 8bit}{8k \times 8bit} = 4.$$

The 8k memory has  $2^3 \cdot 2^{10} = 2^{13}$  memory locations which can be accessed by using 13 address lines ( $A_0, \dots, A_{12}$ ).

The 32k memory has  $2^5 \cdot 2^{10} = 2^{15}$  memory locations which can be accessed by using 15 address lines ( $A_0, \dots, A_{14}$ ). The additional addresses  $A_{14}$  and  $A_{13}$  decoded with a 2:4 DCD are used to enable the 4 semiconductor memories of type 6264 according to the table below.

$A_{14}$	$A_{13}$	$A_{12} - A_0$	Enabled Circuit	Enable conditions			
				$\overline{CE_0}$	$\overline{CE_1}$	$\overline{CE_2}$	$\overline{CE_3}$
0	0	X.....X	0	0	1	1	1
0	1	X.....X	1	1	0	1	1
1	0	X.....X	2	1	1	0	1
1	1	X.....X	3	1	1	1	0

Table12.1 Truth table for the 32kx8bit memory

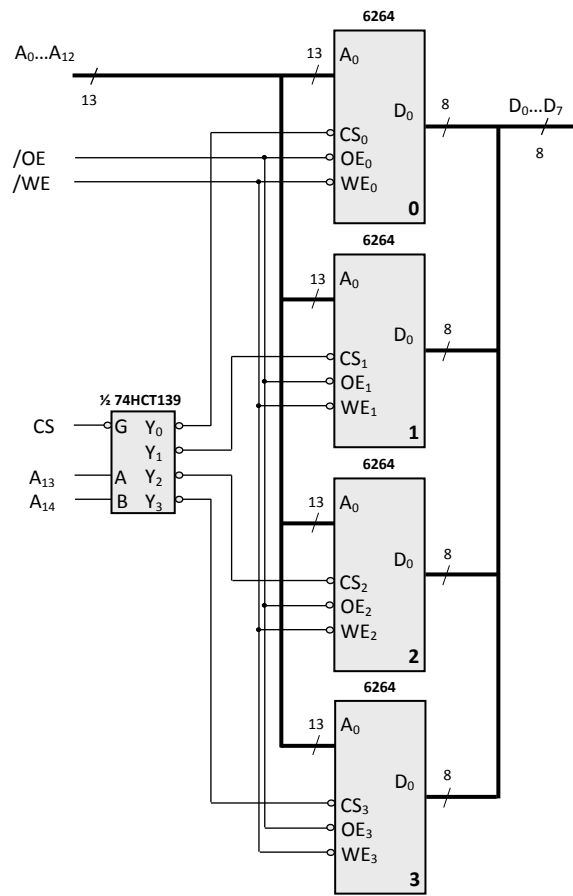
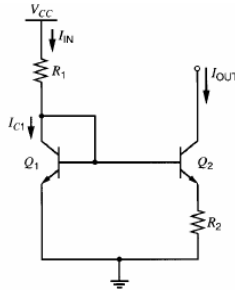


Fig 12.1 A 32k x 8 bit memory built with 4 ICs 6264



## ANALOG INTEGRATED CIRCUITS – 5 THEORY QUESTIONS

### 1. Bipolar Widlar Current Source - draw the schematic, explain why it is not a current mirror.



(Abstract: In the Widlar current source the transistors  $Q_1$  and  $Q_2$  operate with unequal base emitter voltages. This circuit is referred to as a current source rather than a current mirror because the output current,  $I_{OUT}$ , is much smaller than the input current,  $I_{IN}$ .)

Fig. 19.

In the Widlar current source of Fig. 19, the resistor  $R_2$  is inserted in series with the emitter of  $Q_2$ , and transistors  $Q_1$  and  $Q_2$  operate with unequal base emitter voltages if  $R_2 \neq 0$ . This circuit is referred to as a current source rather than a current mirror because the output current is much less dependent on the input current and the power-supply voltage than in the simple current mirror.

Assume that  $Q_1$  and  $Q_2$  operate in the forward active region. KVL around the base-emitter loop gives:

$$V_{BE1} - V_{BE2} - \frac{\beta_F + 1}{\beta_F} I_{OUT} R_2 = 0 \quad \Rightarrow \quad V_T \ln \frac{I_{C1}}{I_{S1}} - V_T \ln \frac{I_{OUT}}{I_{S2}} - \frac{\beta_F + 1}{\beta_F} I_{OUT} R_2 = 0$$

$$\text{If } \beta \rightarrow \infty \text{ and } I_{S1} = I_{S2} \quad \Rightarrow \quad V_T \ln \frac{I_{IN}}{I_{OUT}} = I_{OUT} R_2$$

This transcendental equation can be solved by trial and error to find  $I_{OUT}$  if  $R_2$  and  $I_{IN}$  are known, as in typical analysis problems. Because the logarithm function compresses changes in its argument, attention can be focused on the linear term,  $I_{OUT} R_2$ , simplifying convergence of the trial-and-error process. In design problems, however, the desired  $I_{IN}$  and  $I_{OUT}$  are usually known, and the equations provides the required value of  $R_2$ .

The Widlar source allows currents in the microamp range to be realized with moderate values of resistance. It is possible to write the final equation like this:

$$I_{IN} = I_{OUT} e^{\frac{I_{OUT} R_2}{V_T}}$$

It is obvious that  $I_{OUT}$  is much smaller than  $I_{IN}$ .

Exemple:  $I_{IN} = 1 \text{ mA}$ ,  $R_2 = 5 \text{ K}\Omega$ ,  $I_{OUT} = 20 \text{ }\mu\text{A}$

**2. Temperature-Insensitive Bias with band gap voltage reference: the motive, the idea, one of the practical implementations.**

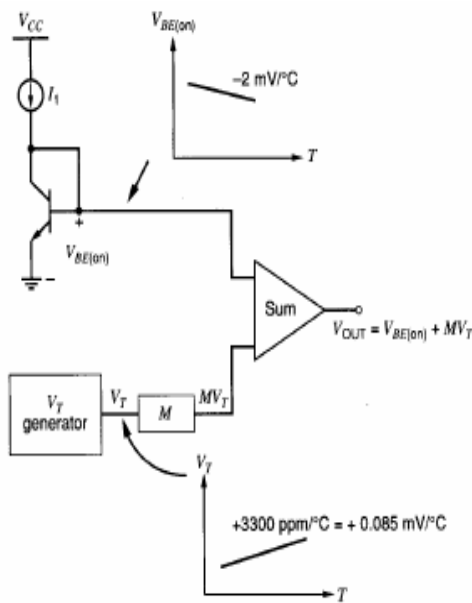


Fig. 20.

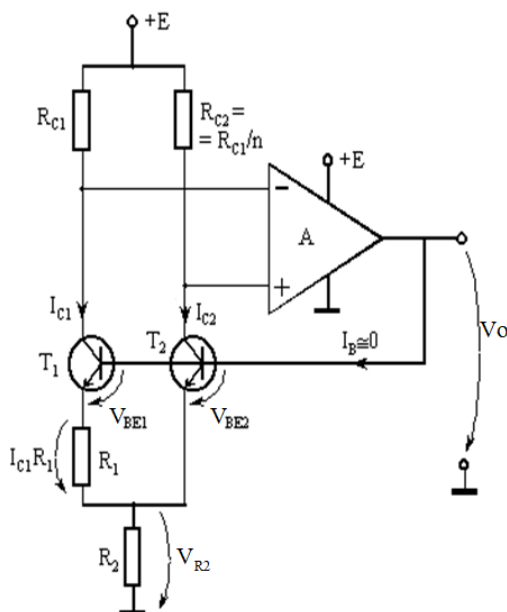
(Abstract: We need low-temperature-coefficient reference voltages. The idea is shown in Fig. 20.  $-2 \text{ mV}/^\circ\text{C}$  temperature-coefficient of  $V_{BE}$  to be compensated with a component with  $+2 \text{ mV}/^\circ\text{C}$  coefficient temperature. )

In practice, requirements often arise for low-temperature-coefficient voltage bias or reference voltages. The voltage reference for a voltage regulator is a good example.

Since  $V_{BE(on)}$  and  $V_T$  have opposite  $T_{CF}$ , the possibility exists for referencing the output current to a composite voltage that is a weighted sum of  $V_{BE(on)}$  and  $V_T$ . By proper weighting, zero temperature coefficient should be attainable. So we can obtain low-temperature-coefficient voltage bias or reference voltages.

$$V_{OUT} = V_{BE(on)} + M V_T$$

The idea is shown in Fig. 20.  $-2 \text{ mV}/^\circ\text{C}$  temperature-coefficient of  $V_{BE}$  to be compensated with a component with  $+2 \text{ mV}/^\circ\text{C}$  coefficient temperature. One possibility is to use  $V_T$  which  $T_{CF}$  is about  $+0,085 \text{ mV}/^\circ\text{C}$ .



A bandgap voltage reference is a voltage reference circuit widely used in integrated circuits usually with an output voltage around 1.25 V, close to the theoretical band gap of silicon at  $0^\circ\text{K}$ . A practical implementation is shown in Fig. 21.

$$\begin{aligned}
 V_{RC1} &= V_{RC2} \Rightarrow I_{C1} = I_{C2} \\
 V_{R1} &= I_{C1} R_1 = V_{BE2} - V_{BE1} = \\
 &= V_T \ln \frac{I_{C2}}{I_S} - V_T \ln \frac{I_{C1}}{I_S} = V_T \ln \frac{I_{C2}}{I_{C1}} = V_T \ln n \\
 V_{R2} &= R_2 (I_{C1} + I_{C2}) = R_2 \left( \frac{V_T \ln n}{R_1} + n \frac{V_T \ln n}{R_1} \right) = \\
 &= \frac{R_2}{R_1} (n + 1) V_T \ln n = N \cdot V_T
 \end{aligned}$$

$$\frac{dV_{R2}}{dT} = N \frac{dV_T}{dT} = N \frac{k}{q} = N \frac{kT}{qT} = N \frac{V_T}{T} = +2 \frac{mV}{^\circ C} \quad \Rightarrow N = 2 \cdot 10^{-3} \frac{300}{26 \cdot 10^{-3}} \cong 23$$

**3. Inverting and noninverting amplifier built with an ideal op amp - draw the schematics and find the gains, define the characteristics of an ideal op amp.**

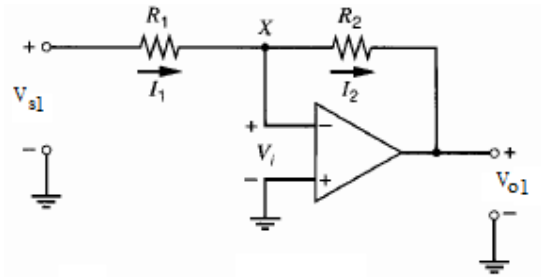


Fig. 22.

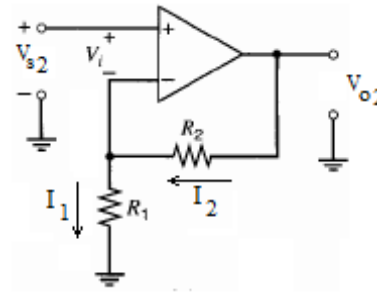


Fig. 23.

$$V_{o1} = -V_{s1} \frac{R_2}{R_1}$$

$$V_{o2} = \left(1 + \frac{R_2}{R_1}\right) V_{s2}$$

(Abstract: The golden rules:

- 1.The output attempts to do whatever is necessary to make the voltage difference between the inputs zero (in Fig. 22 and Fig. 23,  $V_i = 0$ ).
- 2.The inputs draw no current.)

An ideal op amp with a single-ended output has a differential input, infinite voltage open-loop gain, infinite input resistance, and zero output resistance. While actual op amps do not have these ideal characteristics, their performance is usually sufficiently good that the circuit behavior closely approximates that of an ideal op amp in most applications. These characteristics lead to the golden rules for op-amps. They allow us to logically deduce the operation of any op-amp circuit.

Fig. 22 shows an inverting amplifier build with an op amp. Considering we have an ideal op amp. First, because no current enters in the "-" input, at the nod X we can write:

$$I_1 = I_2 \quad (1)$$

Second,  $V_i = 0$  and at the inverting input we have a "virtual ground". Then the voltage  $V_{s1}$  is across  $R_1$  and  $V_{o1}$  is across  $R_2$ . In the first equation we can replace  $I_1$  and  $I_2$  with the values:

$$I_1 = \frac{V_{s1}}{R_1} \quad I_2 = \frac{-V_{o1}}{R_2}$$

Equation (1) becomes:

$$\frac{V_{s1}}{R_1} = -\frac{V_{o1}}{R_2} \Leftrightarrow V_{o1} = -V_{s1} \frac{R_2}{R_1}$$

This is the relationship between the output voltage and the input voltage for an inverting amplifier build with an op amp. A similar calculation can be done for the noninverting amplifier build with an ideal op amp (Fig. 23). The same, for Fig. 23:

$$I_1 = I_2 \quad (2)$$

But we don't have a virtual ground anymore: at the noninverting input is  $V_{s2}$ . In this case we can write:

$$I_1 = \frac{V_{s2}}{R_1} \quad I_2 = \frac{V_{o2} - V_{s2}}{R_2}$$

Using this values in (2) we get the relationship between the output voltage and the input voltage for a noninverting amplifier build with an op amp:

$$\frac{V_{s2}}{R_1} = \frac{V_{o2} - V_{s2}}{R_2} \Leftrightarrow V_{o2} = \left(1 + \frac{R_2}{R_1}\right) V_{s2}$$

**4. Integrator, differentiator build with op amp - draw the schematics, find the relationships between input and output voltages.**

The integrator (Fig. 24) and the differentiator circuits (shown in Fig. 25) are examples of using op amps with reactive elements in the feedback network to realize a desired frequency response or time-domain response.

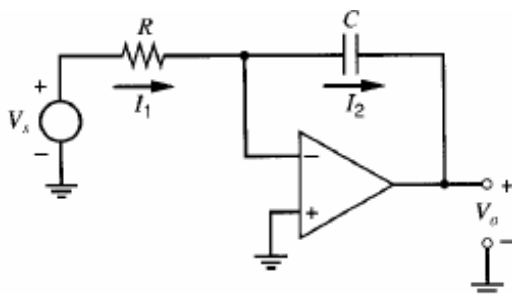


Fig. 24.

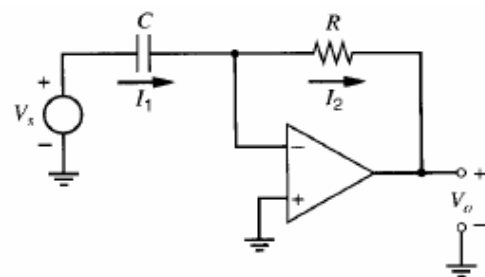


Fig. 25.

**(Abstract:** In the case of the integrator the output voltage is proportional to the integral of the input voltage with respect to time. In the case of the differentiator the output voltage is proportional to the time rate of change of the input voltage.)

In the case of the integrator (Fig. 24), the resistor R is used to develop a current  $I_1$  that is proportional to the input voltage,  $V_s$ . This current flows into the capacitor C, whose voltage is proportional to the integral of the current  $I_2$  with respect to time. Since the output voltage is equal to the negative of the capacitor voltage, the output is proportional to the integral of the input voltage with respect to time. In terms of equations:

$$I_1 = \frac{V_s}{R} = I_2 \quad V_o = -\frac{1}{C} \int_0^t I_2 d\tau + V_o(0) \Rightarrow V_o(t) = -\frac{1}{RC} \int_0^t V_s(\tau) d\tau + V_o(0)$$

In the case of the differentiator (Fig. 25), the capacitor C is connected between  $V_s$  and the inverting op-amp input. The current through the capacitor is proportional to the time derivative of the voltage across it ( $V_c$ ), which is equal to the input voltage ( $V_c = V_s$ ). This current flows through the feedback resistor R, producing a voltage at the output proportional to the capacitor current, which is proportional to the time rate of change of the input voltage. In terms of equations:

$$I_1 = C \frac{dV_s}{dt} = I_2 \quad V_o = -RI_2 = -RC \frac{dV_s}{dt}$$

**5. Improved precision half-wave rectifier - draw the schematic, the equivalent ones, the diadrames and explain the operation.**

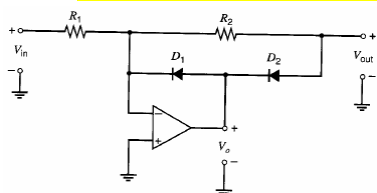


Fig. 26.

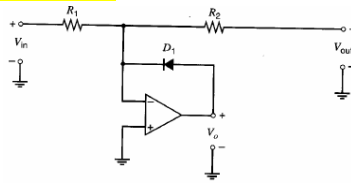


Fig. 27.

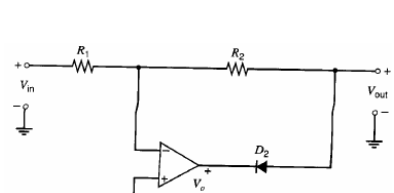


Fig. 28.

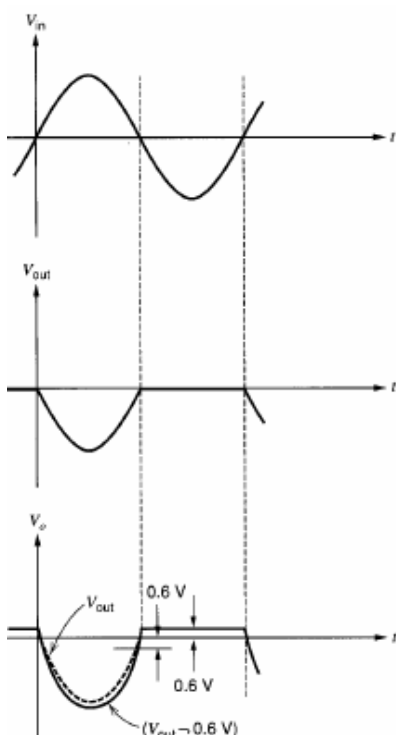


Fig. 29.

(Abstract: The schematic for an improved precision half-wave rectifier is shown in Fig. 26. Fig. 27 shows the equivalent circuit for  $V_i < 0$  and Fig. 28 shows the equivalent circuit for  $V_i > 0$ . Fig. 29 shows the waveforms within the improved precision rectifier for a sinusoidal input,  $V_{in}$ ; the output of the circuit is  $V_{out}$  and  $V_o$  is the op amp's output.)

For input voltages less than zero, the equivalent circuit is shown in Fig. 27. Diode  $D_1$  is forward biased and the op amp is in the active region. The inverting input of the op amp is clamped at ground by the feedback through  $D_1$ , and, since no current flows in  $R_2$ , the output voltage is also at ground. When the input voltage is made positive, no current can flow in the reverse direction through  $D_1$  so the output voltage of the op amp  $V_o$  is driven in the negative direction. This reverse biases  $D_1$  and forward biases  $D_2$ . The resulting equivalent circuit is shown in Fig. 28 and is simply an inverting amplifier with a forward-biased diode in series with the output lead of the op amp.

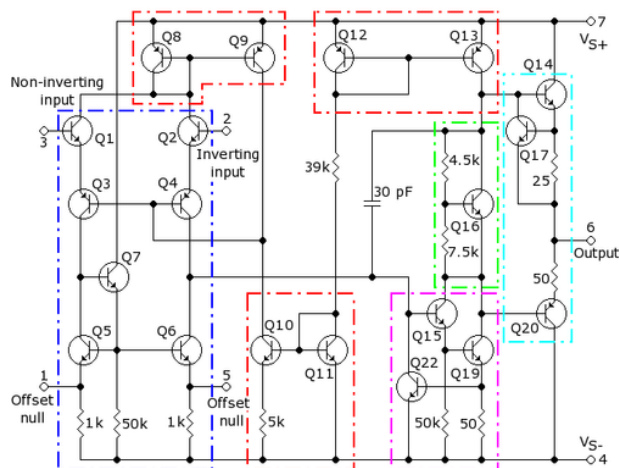
Because of the large gain of the op amp, this diode has no effect on its behavior as long as it is forward biased, and so the circuit behaves as an inverting amplifier giving an output voltage of:

$$V_{out} = -\frac{R_2}{R_1} V_{in}$$

As shown in Fig. 29, the output voltage of the operational amplifier need only change in value by approximately two diode drops when the input signal changes from positive to negative.

## Analog Integrated Circuits – 2 problems

**Problem #1.** Name the building blocks inside the op amp shown in the figure.



Problem #1. ANSWER

1. At the left-hand side of the figure, the first block is a differential input stage with emitter followers (Q1 and Q2) driving common-base stages (Q3 and Q4).

The transistors Q5 and Q6 form an active load for Q3 and Q4.

Q7, Q5, Q6 and their emitter resistances form a current mirror with degeneration.

The two pairs of transistors shown at the top of the schematic are simple current mirrors (Q8 and Q9, Q12 and Q13).

At the bottom is a Widlar current source (built with Q10, Q11, and the 5 kΩ resistor).

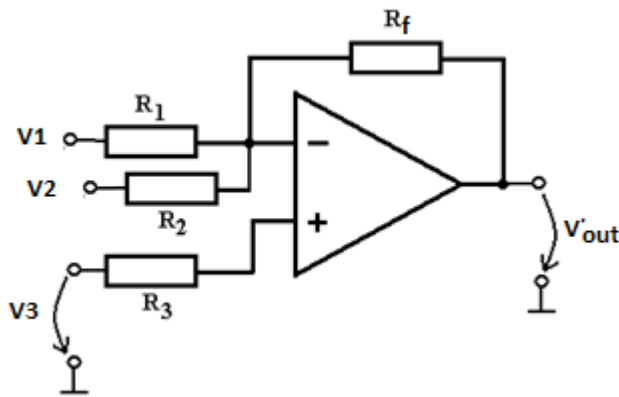
Transistors Q15, Q19 and Q22 operate as a class A gain stage. The stage consists of two NPN transistors in a Darlington configuration (Q15 and Q19).

Transistor Q16 and its base resistors is the  $V_{be}$  multiplier voltage source.

Transistors Q14, Q20 form the class AB push-pull emitter follower output stage.

**Problem #2.**

**Problem 4.8. Design an amplifier in order to obtain an output voltage equal to  $V_{out} = -V_1 - 2V_2 + 5V_3$ . Consider  $R_f = 10K\Omega$ .**



**Solution:**

a). An amplifier build with an op amp will be drawn (fig. 2.1):

$$V'_{out} = -V_1 \frac{R_f}{R_1} - V_2 \frac{R_f}{R_2} + V_3 \left( 1 + \frac{R_f}{R_1 \parallel R_2} \right)$$

In order to check if the schematic is correct, we determin the resistor's value by identifying the coefficients.

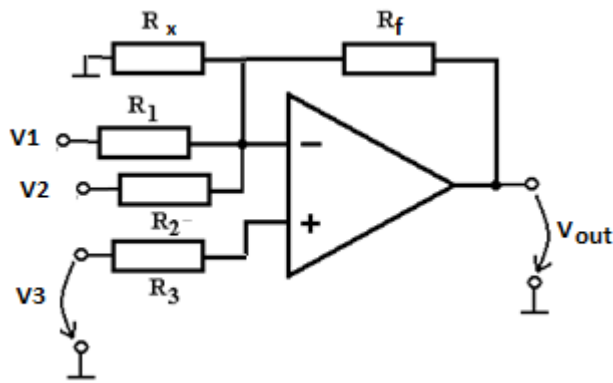
$$\frac{R_f}{R_1} = 1 \Rightarrow R_1 = 10K\Omega; \quad \frac{R_f}{R_2} = 2 \Rightarrow R_2 = 5K\Omega$$

We check the coefficient of  $V_3$ : 
$$1 + \frac{R_f}{R_1 \parallel R_2} = 1 + \frac{10}{\frac{10 \cdot 5}{10 + 5}} = 1 + \frac{10}{\frac{50}{3}} = 4$$

Because  $4 < 5$  we must increase this coefficient  $\left( 1 + \frac{R_f}{R_1 \parallel R_2} \right)$ ! It can be done by adding a

supplementary resistor at the inverting input. The ratio  $\frac{R_f}{R_1 \parallel R_2}$  will increase because the

denominator will decrease:  $\frac{R_f}{R_1 \parallel R_2 \parallel R_x}$ .



$$V_{out} = -V_1 \frac{R_f}{R_1} - V_2 \frac{R_f}{R_2} + V_3 \left( 1 + \frac{R_f}{R_1 \parallel R_2 \parallel R_x} \right)$$

Now we identify the coefficients to find the value for Rx:

$$\left( 1 + \frac{R_f}{R_1 \parallel R_2 \parallel R_x} \right) = 5 \Leftrightarrow \frac{R_f}{R_1 \parallel R_2 \parallel R_x} = 4$$

$$\Rightarrow R_x = 10K\Omega$$

We determine R3 from MEC relationship:  $R_1 \parallel R_2 \parallel R_f \parallel R_x = R_3 \Rightarrow R_3 = 5K\Omega$

## SIGNAL PROCESSING

### References

[1] Corina Nafornitã, Alexandru Isar, Signals and Systems, vol. II, Editura Politehnica, Timișoara, 2016.

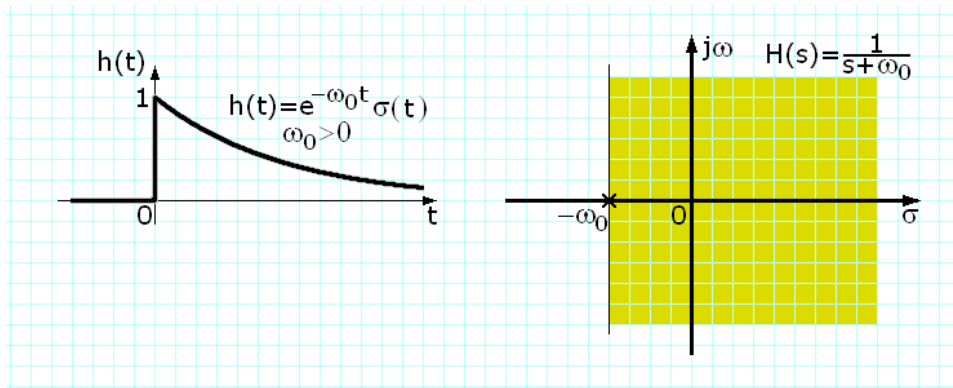
### 1-Where are the poles of a stable and causal analog system? Give an example.

The poles of a stable and causal system are located in the left half plane LHP while its zeros can be located anywhere in the complex plane. Example:  $h(t) = \exp(-\omega_0 t) \sigma(t), \omega_0 > 0$ .

[1] -page 110

The transfer function is  $H(\omega) = \frac{1}{s + \omega_0}$  with one pole,  $s_p = -\omega_0$ .





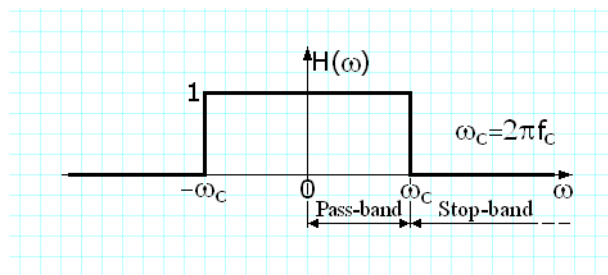
**2-Ideal low pass filter. Frequency response and impulse response. Is this filter realizable?**

[1]-page 134

The ideal low pass filter has the frequency response:

$$H(\omega) = p_{\omega_c}(\omega) \leftrightarrow h(t) = \frac{\sin \omega_c t}{\pi t}$$

It does not fulfill Paley-Wiener theorem, so it is not causal.



**3-Enunciate WKS sampling theorem.**

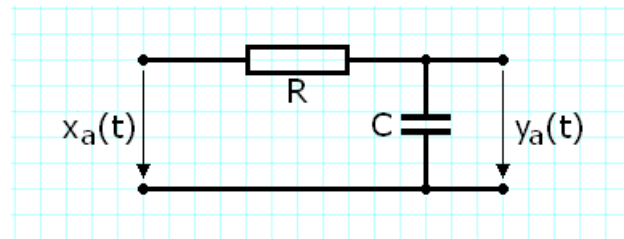
[1]-page 150

If the finite energy signal  $x(t)$  is band limited at  $\omega_M$ , ( $X(\omega)=0$  for  $|\omega| > \omega_M$ ), it is uniquely determined by its samples  $\{x(nT_s) | n \in \mathbf{Z}\}$  if the sampling frequency is higher or equal than twice the maximum frequency of the signal:

$$\omega_s \geq 2\omega_M$$

#### 4-Approximation of RC circuit using bilinear transform method.

[1]-page 265



$$\text{time constant: } \tau = RC = \frac{1}{\omega_0}; \quad H_a(s) = \frac{1}{1 + s\tau}$$

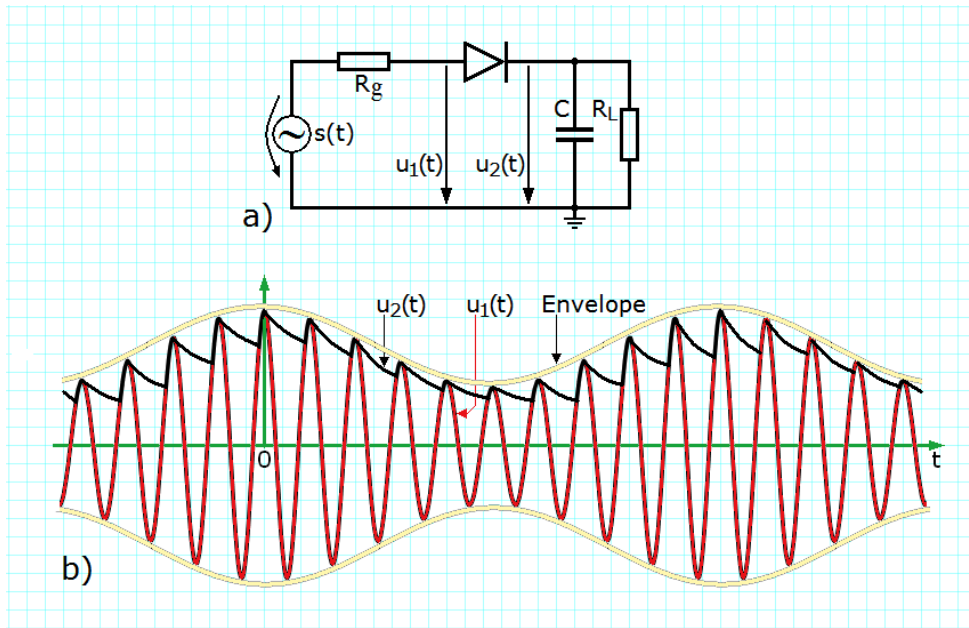
$$s = \frac{2}{T} \frac{1 - z^{-1}}{1 + z^{-1}}; \quad H_d(z) = H_a(s) \Big|_{s = \frac{2}{T} \frac{1 - z^{-1}}{1 + z^{-1}}}$$

$$\Rightarrow H_d(z) = \frac{\frac{T}{T + \tau}}{1 - \frac{\tau}{T + \tau} z^{-1}}$$

#### 5-Demodulator (envelope detector) for AM signals.

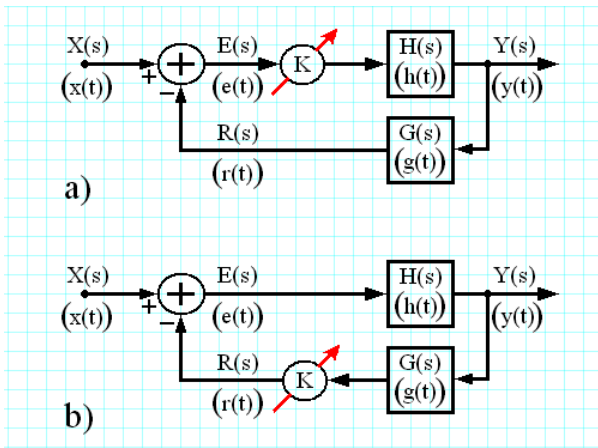
[1]-page 275

AM demodulation can be realized using an envelope detector. For  $R_g \ll R_L$ , the voltage from the capacitor  $u_2(t)$  follows the voltage  $u_1(t)$  if the latter is high enough and the diode conducts (on the positive half-cycle of the input signal). When the diode becomes reverse biased, the capacitor discharges through the resistor  $R_L$ . The modulating wave is reconstructed using low pass filtering and removal of the DC component for  $u_2(t)$ .



**5-Nyquist stability criterion for continuous-time systems when the open loop system is stable (schema + enunciation).**

[1]-page 350, page 372



$$a) \frac{Y(s)}{X(s)} = \frac{KH(s)}{1 + KH(s)G(s)}$$

$$b) \frac{Y(s)}{X(s)} = \frac{H(s)}{1 + KH(s)G(s)}$$

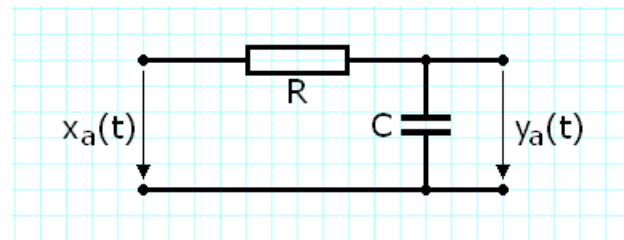
**-If the open loop system is stable then  $H(s)G(s)$  doesn't have poles in the right half plane or on the imaginary axis. So, the open loop Nyquist's hodograph**

$G(j\omega)H(j\omega)$  **doesn't encircle** the critical point  $(-1/K, 0)$

-Since  $h(t)$  and  $g(t)$  are real functions, Nyquist's hodograph for  $\omega \in (-\infty, 0)$  is obtained by **symmetry** with respect to the real axis of the complex plane  $H(s)G(s)$  from the Nyquist's hodograph for  $\omega \in (0, \infty)$

**Problem 1- What is the transfer function of a digital system obtained using the bilinear transform method, from a lowpass RC circuit, with  $R= 1 \text{ k}\Omega$  and  $C = 1 \text{ }\mu\text{F}$ , considering that the sampling step is  $500 \text{ }\mu\text{s}$  ?**

[1]-page 265



The time constant of this circuit is  $RC$  , inversely proportional with the cutoff frequency,  $\omega_0$  :  
 $\tau = RC = 1 \text{ ms}$ ,  $\omega_0 = 1/RC = 1000 \text{ rad/s}$  .

The transfer function of the analog LTI system is  $H_a(s) = \frac{1}{1+s\tau}$  . For the bilinear transform we

replace  $s = \frac{2}{T} \frac{1-z^{-1}}{1+z^{-1}}$  in the transfer function, so we have  $H_d(z) = H_a(s) \Big|_{s = \frac{2}{T} \frac{1-z^{-1}}{1+z^{-1}}}$  where  $T$  is the

sampling step.

For the lowpass RC circuit we obtain the transfer function:

$$H_d(z) = \frac{\frac{T}{T+\tau}}{1 - \frac{\tau}{T+\tau} z^{-1}} = \frac{\frac{0,5}{1,5}}{1 - \frac{1}{1,5} z^{-1}} = \frac{0,5}{1,5 - z^{-1}} .$$

## Problem 2

**What is the expression of a narrow band frequency modulated signal. Give the implementation of a narrowband modulator, with the carrier  $A_c \cos \omega_c t$ ,  $A_c = 100 \text{ mV}$ ,  $\omega_c = 2 \cdot 10^6 \cdot \pi \text{ rad/s}$  and the modulating wave  $A_m \cos \omega_m t$ ,  $A_m = 10 \text{ mV}$ ,  $\omega_m = 2 \cdot 10^3 \cdot \pi \text{ rad/s}$  .**

[1]-page 298

FM signal's expression is:  $s(t) = A_c \cos \theta_i(t) = A_c \cos[\omega_c t + \beta \sin \omega_m t]$ , where the modulating wave to be transmitted is  $x(t) = A_m \cos \omega_m t$ . Depending on the value of the modulation index  $\beta = \Delta\omega / \omega_m$ , we have narrow band FM ( $\beta \ll 1$  radian) or wide band FM ( $\beta \gg 1$  radian). For narrow band FM, the modulated wave is:

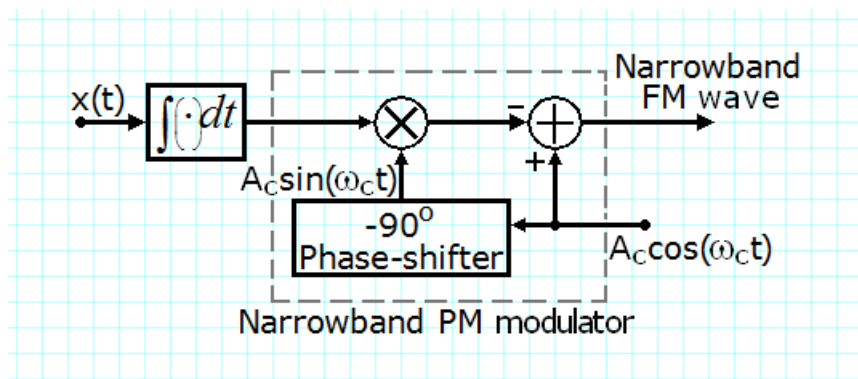
$$s(t) = A_c \cos \omega_c t \cos(\beta \sin \omega_m t) - A_c \sin \omega_c t \sin(\beta \sin \omega_m t).$$

$$\text{If } \beta < \frac{\pi}{36} \text{ rad} \Rightarrow \cos(\beta \sin \omega_m t) \cong 1 \text{ and } \sin(\beta \sin \omega_m t) \cong \beta \sin \omega_m t$$

$$\Rightarrow s(t) = A_c \cos \omega_c t - \beta A_c \sin \omega_c t \sin \omega_m t. \quad (1)$$

This is the narrow band FM signal's expression.

A possible implementation scheme is shown below.



One input of the FM modulator is the modulating wave  $x(t)$  and the other input is the carrier  $A_c \cos \omega_c t$ , the first term in the narrow band FM signal. Through its phase shift of  $-90^\circ$  we obtain the signal  $A_c \sin \omega_c t$  which is multiplied with the integrated modulating wave:  $\frac{A_m}{\omega_m} \sin \omega_m t$ , thus obtaining the second term  $\frac{A_c A_m}{\omega_m} \sin \omega_c t \sin \omega_m t$ . Comparing this expression with the second term of the right hand side of relation (1) we can identify the value of the modulation index:

$$\beta = \frac{A_m}{\omega_m} = \frac{10^{-2}}{2\pi \cdot 10^3} \ll 1.$$

This is indeed a narrow band FM.

At the output a narrow band FM signal is obtained.

## ELECTRONIC INSTRUMENTATION

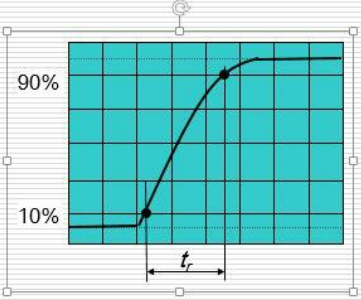
**Oscilloscope** - Relationship between bandwidth and rise time of an oscilloscope. Relationship between rise time of an oscilloscope and rise time of a pulse.

**Solution:**

General purpose analog oscilloscopes

---

Oscilloscope's rise time



Relationship  
between bandwidth  
and rise time

$$t_r(\text{ns}) = \frac{350}{B(\text{MHz})}$$

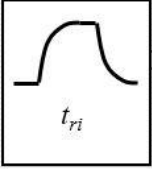
**Exercise** Determine the rise time of a 50 MHz oscilloscope.  
(Answer: 7 ns)

19

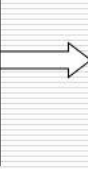
General purpose analog oscilloscopes

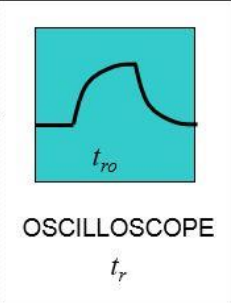
---

Oscilloscopes distort pulse edges !!!



$t_{ri}$





OSCILLOSCOPE

$t_r$

$$t_{ro}^2 = t_{ri}^2 + t_r^2$$

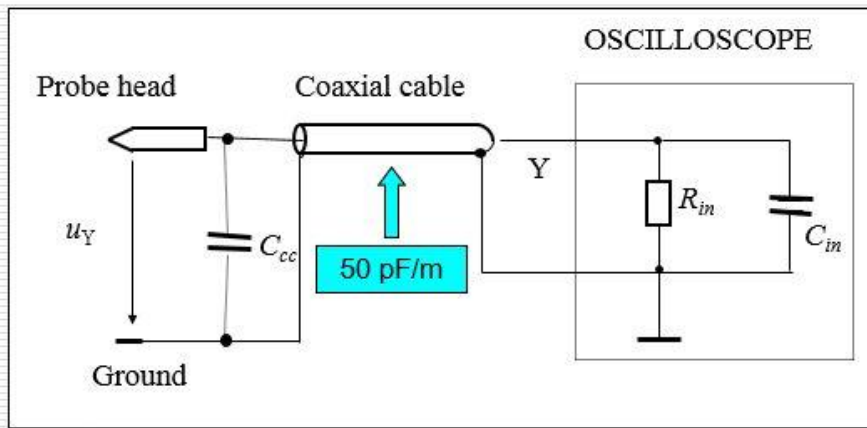
If  $t_{ri} : t_r \geq 5$ , then  $t_{ro} \cong t_{ri}$   
 If  $t_r : t_{ri} \geq 5$ , then  $t_{ro} \cong t_r$

20

**Oscilloscope** - Probes for oscilloscopes without and with attenuator – equivalent circuit, relationships, comparison

**Solution:**

### Passive probe without attenuator



$$R_i = R_{in}$$

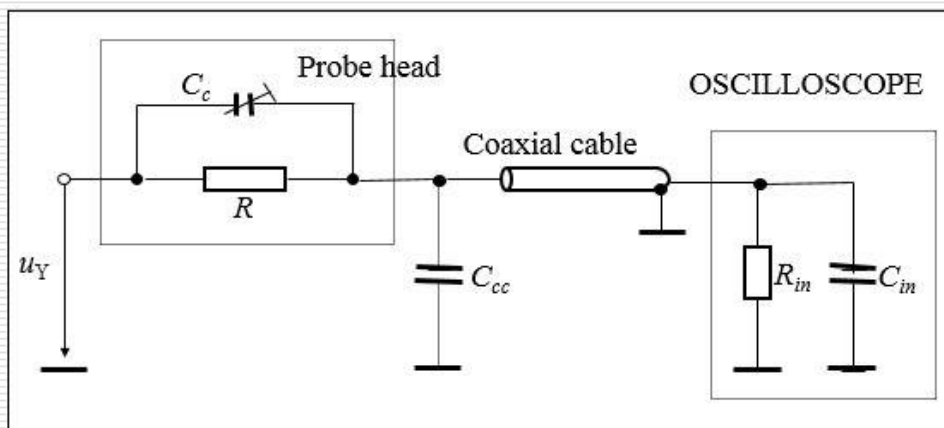
$$C_i = C_{in} + C_{cc}$$

25

Advantage – it does not attenuate the input signal

Disadvantage – relatively small input resistance (1 MΩ), large input capacitance (50 - 150 pF)

### Passive probe with attenuator (in the probe head)



$$R_i = R + R_{in}$$

$$C_i = \frac{C_c \cdot (C_{in} + C_{cc})}{C_c + C_{in} + C_{cc}}$$

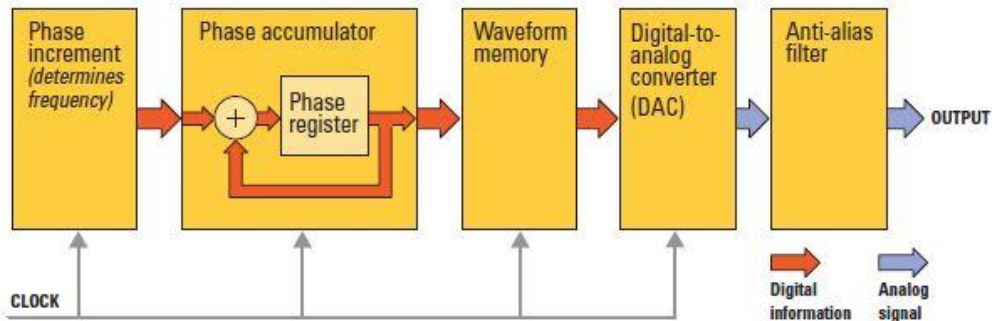
26

Advantage – large input resistance (10 MΩ), small input capacitance (5 - 15 pF)

Disadvantage – it attenuates the input signal (therefore, the value read on the display must be multiplied by the probe's attenuation factor)

## Signal generators. Principle of a Direct Digital Synthesis generator – block diagram, advantages and disadvantages.

### Solution:



DDS (direct digital synthesis) is a technique used in function/arbitrary waveform generators to produce an analog waveform, such as a sine wave. Involve generating a time-varying signal represented in a digital format and then performing a digital-to-analog conversion to convert the digital data into an analog output.

With DDS technology, one cycle of the desired waveform is represented digitally in waveform memory. The contents of the waveform memory are read sequentially. The digital data are representing the desired waveform and are converted by the digital-to-analog converter (DAC). The converter output is a series of voltage steps closely approximating the desired waveform. This is applied to a low-pass anti-aliasing filter to smooth the voltage steps and produce the final output waveform.

DDS methodology sequentially reads waveform memory by using a high-resolution phase accumulator to drive the address input of the waveform memory. On every system clock pulse, the digital value in the phase accumulator is determined by adding a constant digital value, called the phase increment, to the phase accumulator's present value. The most significant bits of the phase accumulator's present value are clocked into the address input of the waveform memory. As a result, the phase increment determines how quickly the values in waveform memory are accessed. This determines the frequency of the output waveform.

The main performance advantages of using DDS technology are:

- Waveform frequency changes are phase-continuous
- Waveform frequency changes are very fast without unwanted effects
- Frequency resolution is digitally controlled and very good ( $\mu\text{Hz}$ )
- Frequency modulation, phase modulation, and frequency sweeps are easily implemented
- Many of the problems associated with analog architectures are eliminated due to the digital nature of DDS

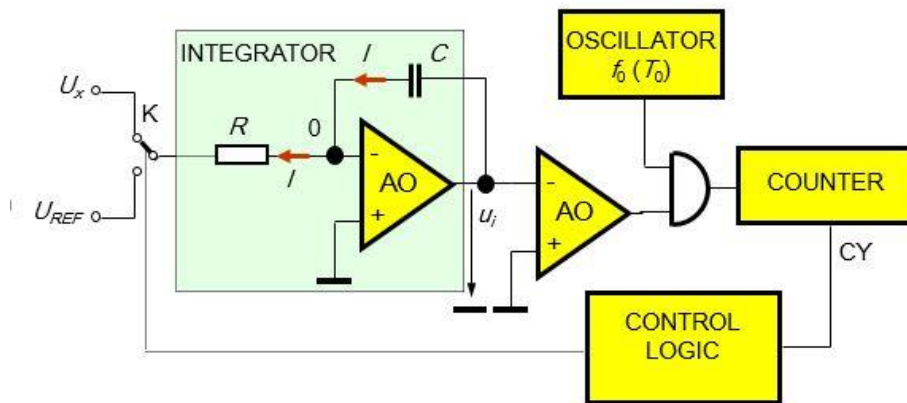
A few significant disadvantages:

- The number of points in a waveform must be equal to an exact power of two
- Increased waveform jitter and distortion are possible



## Digital voltmeters and multimeters. Dual slope ADC – block diagram, operation principle, relationships

**Solution:**



Operation of the converter comprises two steps (phases): (1) integration of the unknown input voltage and (2) integration of a known reference voltage, of opposite polarity. Phase 1 has a fixed duration, denoted  $T_1$ . At the end of this phase, the integrator's output voltage is the same as the voltage across the capacitor. The second phase starts at  $t = T_1$ . Switch K now feeds the reference voltage  $U_{REF}$  at the integrator's input. This leads to the so called de-integration and it ends when the integrator's output nulls.

$$U_{i \max} = \frac{U_x}{RC} T_1$$

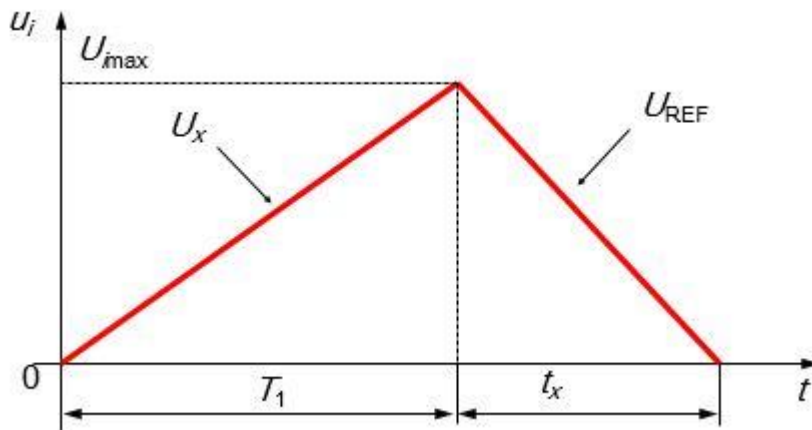
$$T_1 = N \cdot T_0$$

$$U_{i \max} = \frac{U_{REF}}{RC} t_x$$

$$t_x = n \cdot T_0$$

$$U_x \cdot T_1 = U_{REF} \cdot t_x$$

$$U_x = \frac{n}{N} U_{REF}$$



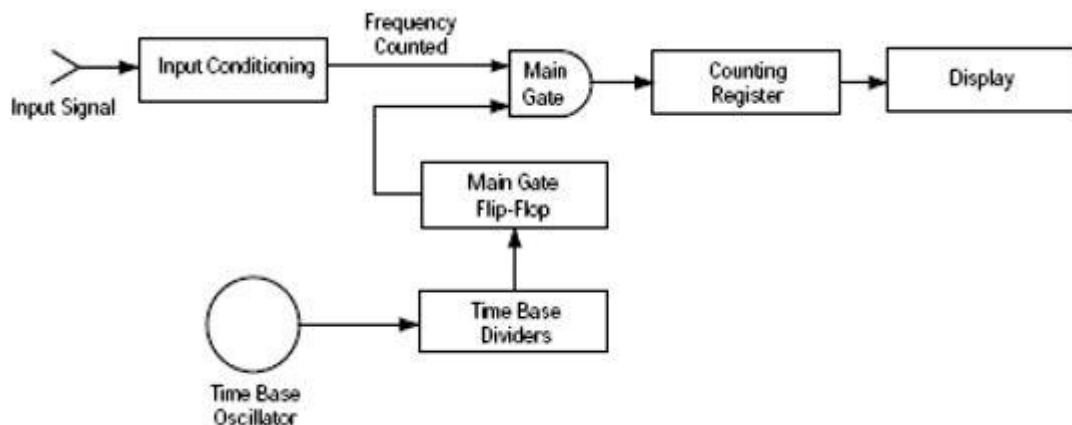
**Universal counters.** Describe the operating principle and explain how frequency can be measured.

**Solution:**

The frequency  $f$  of a repetitive signal can be defined by the number of cycles of that signal per unit of time:  $f=n/t$ , where  $n$  is the number of cycles and  $t$  is the time interval in which they occur. As suggested by the above equation, the frequency can be measured by counting the number of cycles and dividing it by  $t$ .

By taking  $t$  equal to one second, the number of counted cycles will represent the frequency (in Hz) of the signal.

Block diagram of a universal counter in the frequency measurement mode:

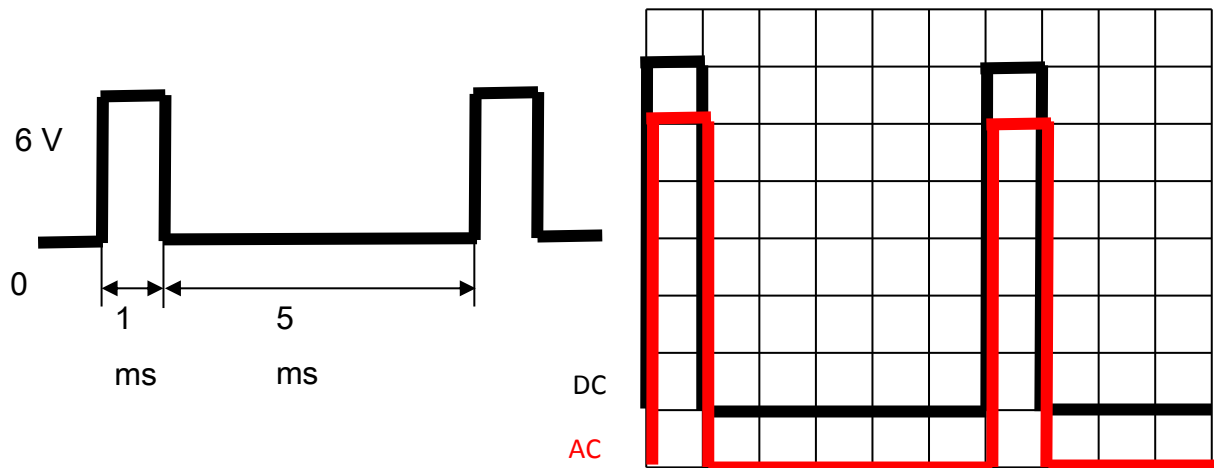


The input signal is initially conditioned to a form that is compatible with the internal circuitry of the counter. The conditioned signal is a pulse train where each pulse corresponds to a cycle of the input signal. With the main gate open, pulses are allowed to pass through and get totalized by the counting register.

The time base oscillator together with the decade dividers and the main gate flip flop control the opening time of the main gate.

If  $T_2=1s$ , the counting register will read the frequency of the input signal (measurement resolution of 1 Hz).

**Oscilloscope – exercise.** Draw the images that appear on the screen if the signal from the figure is applied at the oscilloscope input for 2 cases: DC coupling and AC coupling. Oscilloscope switches are positioned to 1 V / div and 1 ms / div. The screen has 10 divisions on the horizontal and 8 vertical. Zero level is set to three divisions under the horizontal symmetry axis and the time base is internally triggered on positive edge.



**Solution:**

Amplitude  $A=6V$ ,  $1V/div \Rightarrow 6$  divisions

Period  $T=6$  ms,  $1ms/div \Rightarrow 6$  divisions

Pulse width  $t=1$  ms,  $1ms/div \Rightarrow 1$  division

On DC coupling, time base is internally triggered on positive edge – the pulse starts with positive edge, from zero level up to 6 divisions, pulse width 1 division, goes to zero level for 5 divisions and repeats itself.

On AC coupling – DC component is removed - the pulse goes under zero with a value equal to the DC component:

$$U_{DC} = \frac{1}{T} \int_0^T x(t) dt = \frac{1}{T} \int_0^t A dt = 1V$$

$\Rightarrow$  the pulse goes 1 division under zero

**Digital voltmeters and multimeters - exercise.** Specify the measurement result for a 100% confidence level (result  $\pm$

uncertainty, confidence level) according to the rules for data presentation when measuring a voltage of 12.45 V with a 3 ½ digit 20 V voltmeter whose maximum permissible error is given by  $\Delta_t = 0,1\% \times \text{reading} + 0,05\% \times \text{range} + 1 \text{ digit}$ .

**Solution tips:**

The DVM reads xx.xx V. Therefore,

1 digit = 10 mV.

The maximum permissible error when measuring 12.45 V is

$$\Delta_t = 0,1\% \times 12.45 \text{ V} + 0,05\% \times 20 \text{ V} + 10 \text{ mV},$$

or

$$\Delta_t = 12.45 \text{ mV} + 10 \text{ mV} + 10 \text{ mV} = 32.45 \text{ mV}.$$

For a confidence level of 100%, the measurement result should be specified as

$$U = 12.45 \text{ V} \pm 0.03 \text{ V}$$